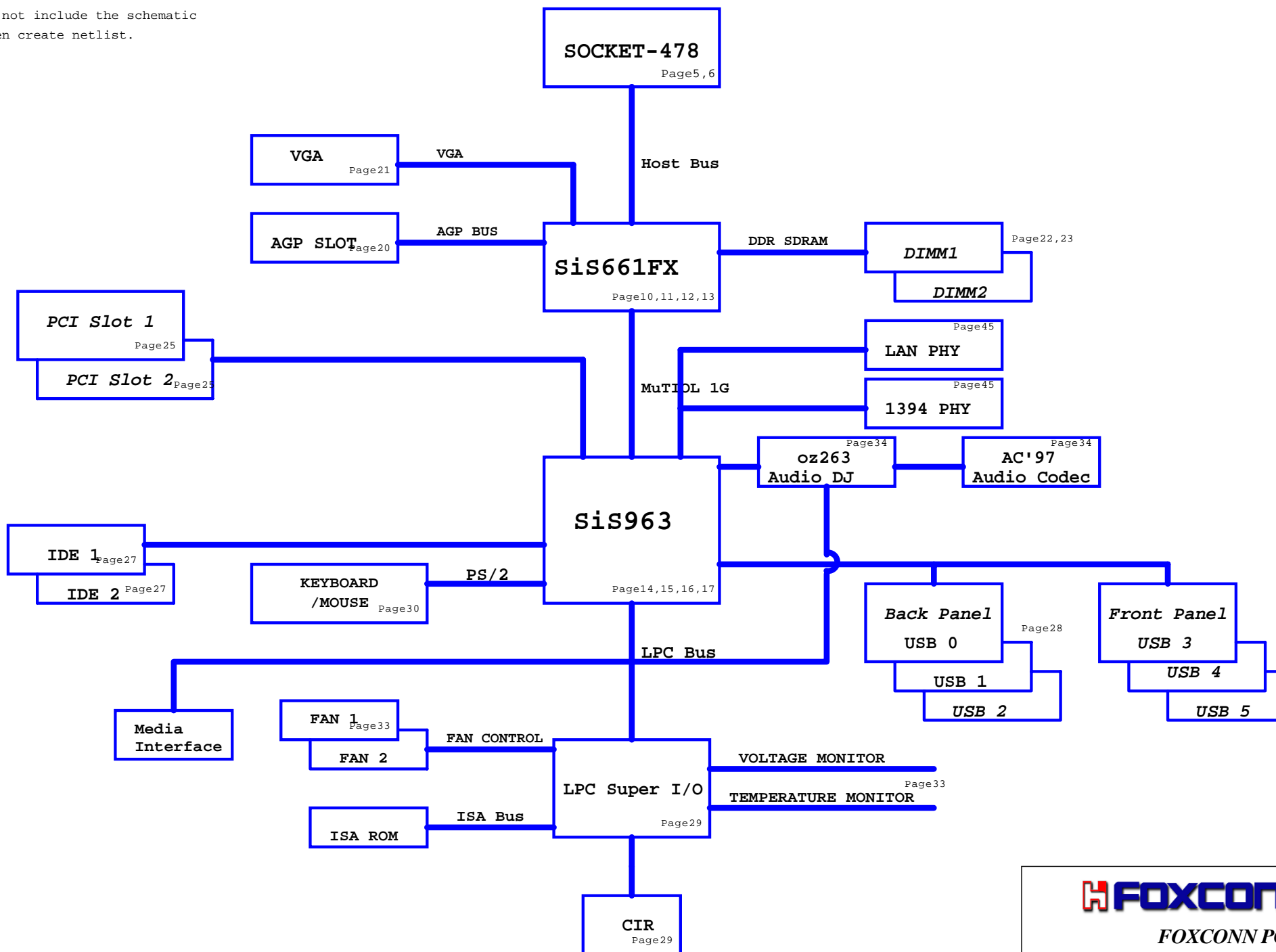
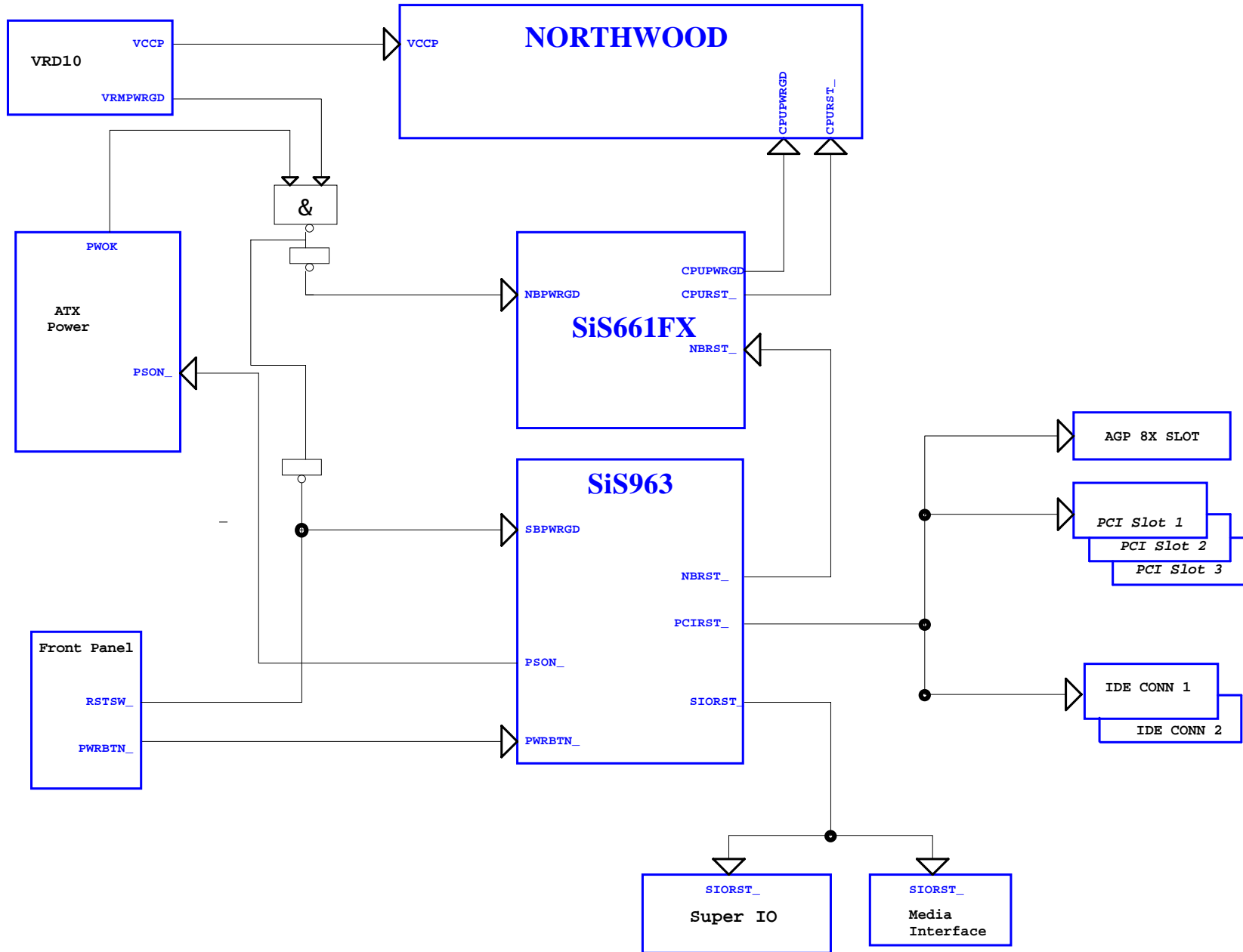
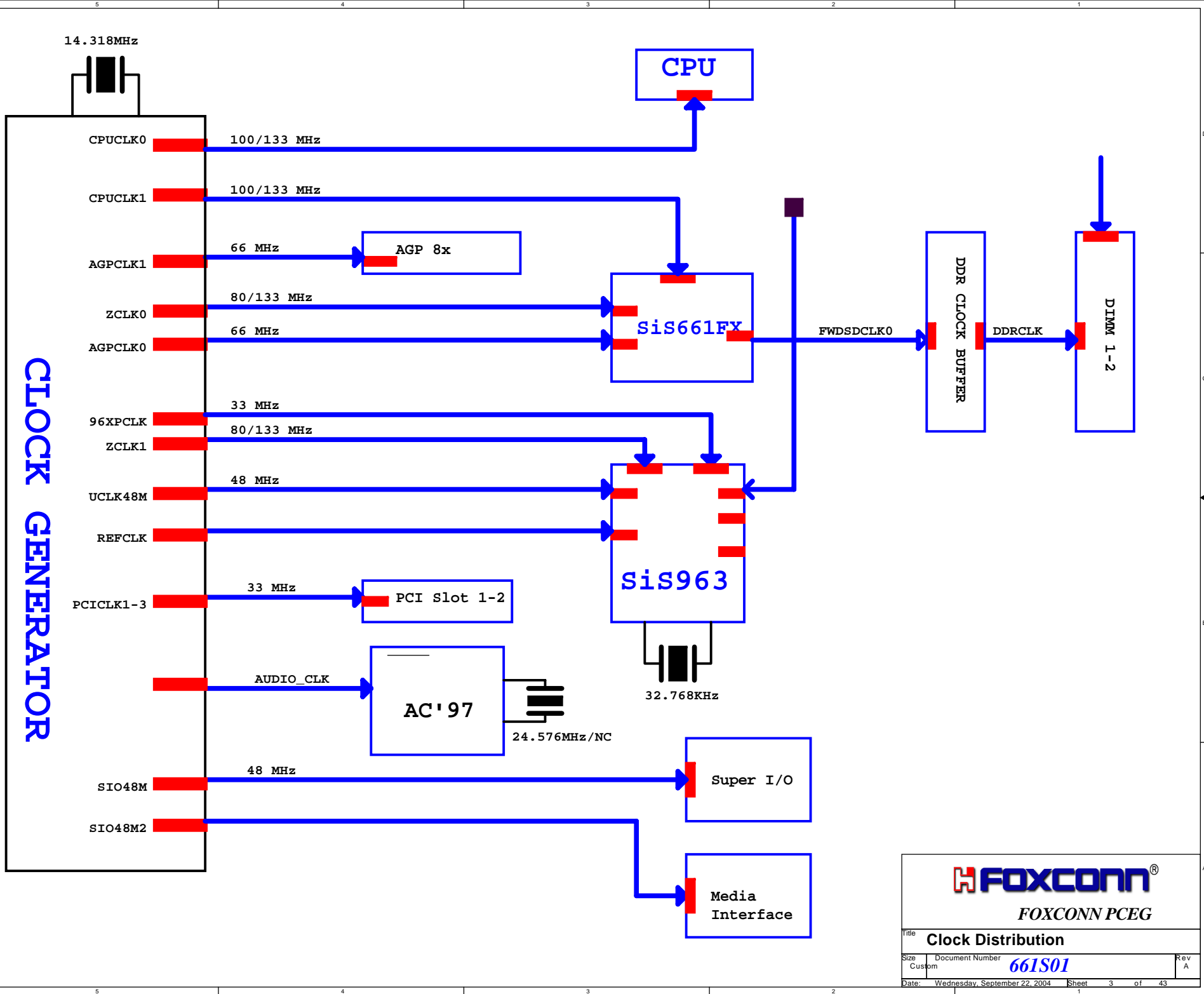


Note:
Do not include the schematic
when create netlist.







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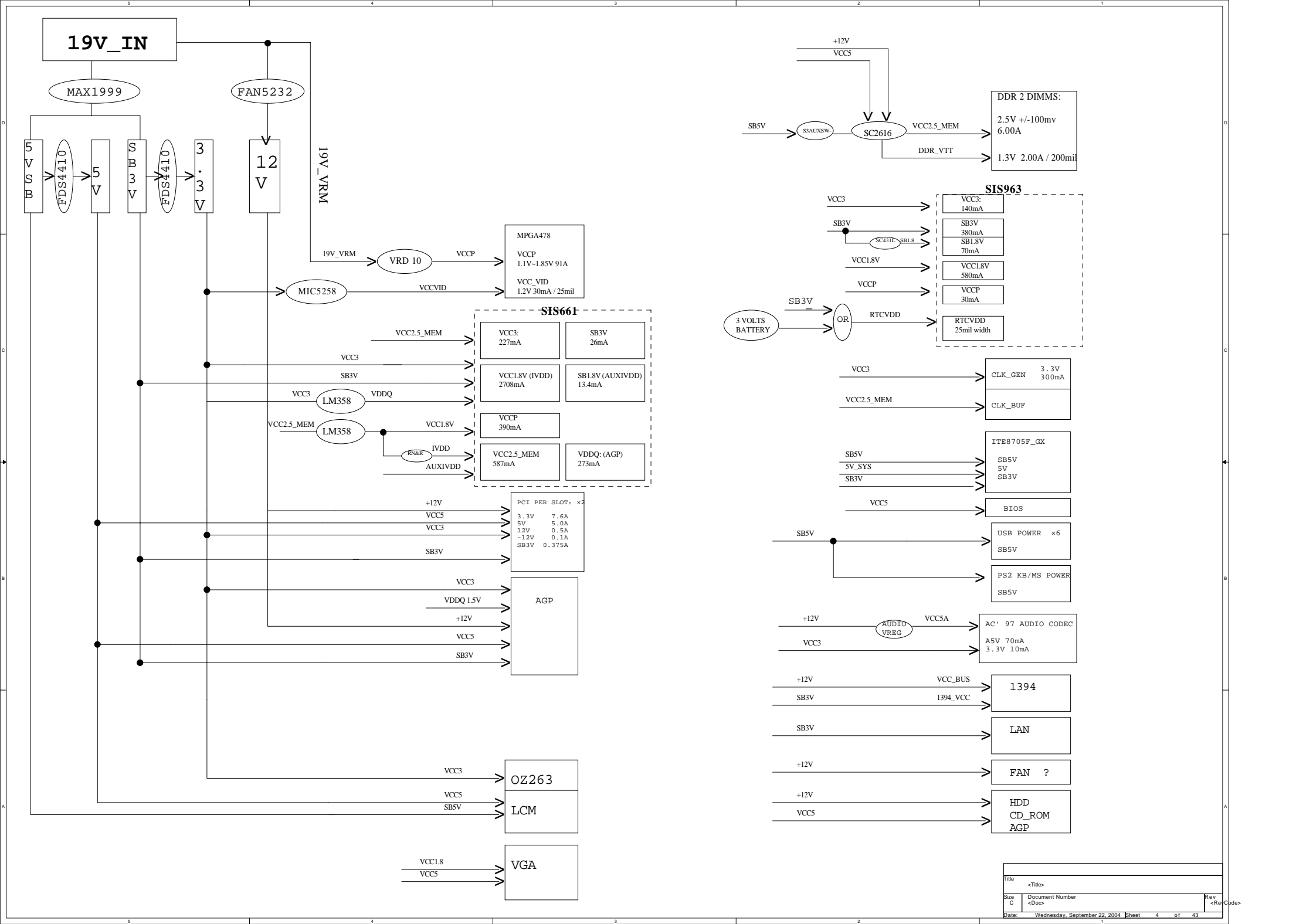
FOXCONN PCEG

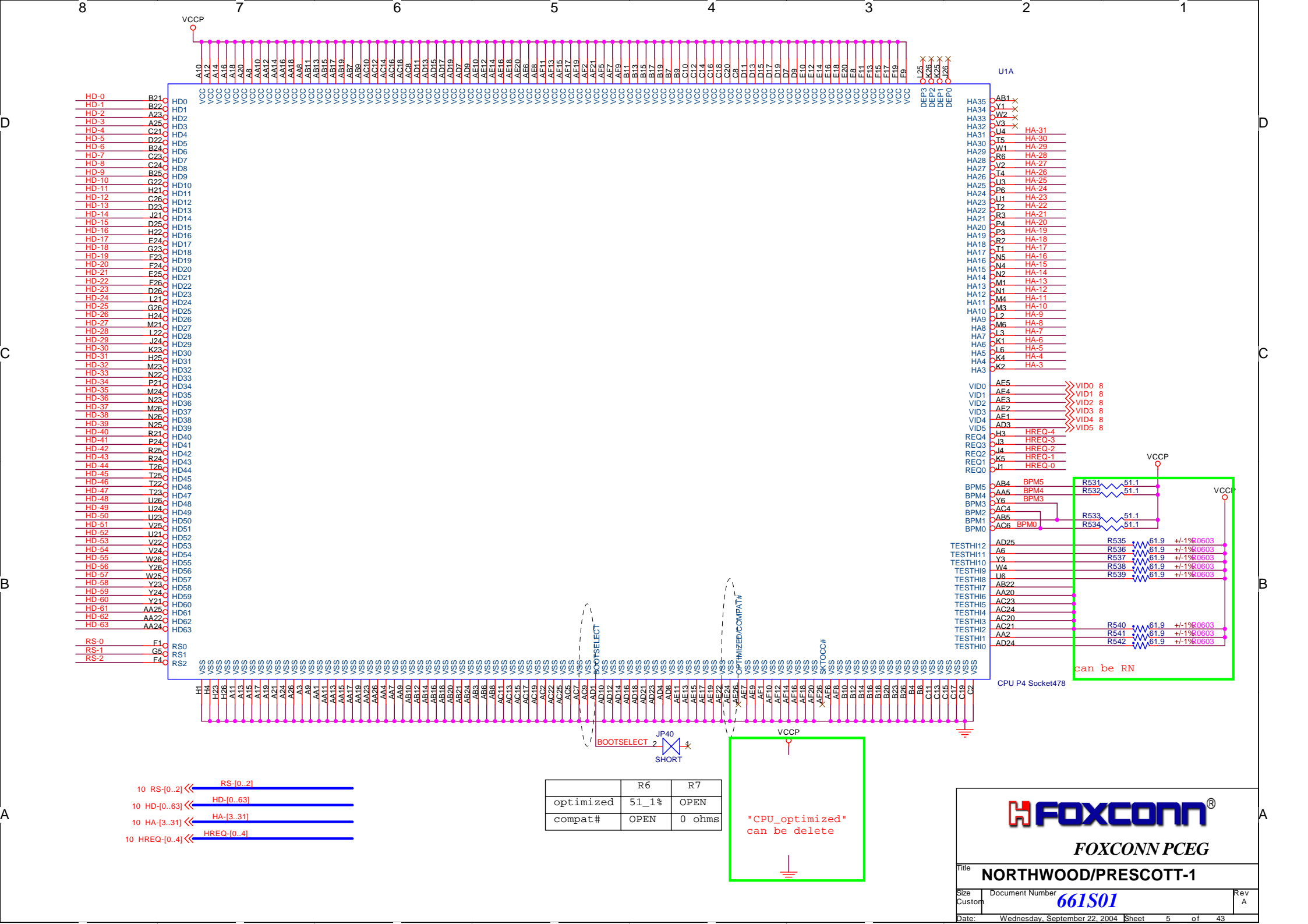
Title **Clock Distribution**

Size Custom Document Number **66IS01**

Rev A

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10 RS-[0..2] << RS-[0..2]
10 HD-[0..63] << HD-[0..63]
10 HA-[3..31] << HA-[3..31]
10 HREQ-[0..4] << HREQ-[0..4]

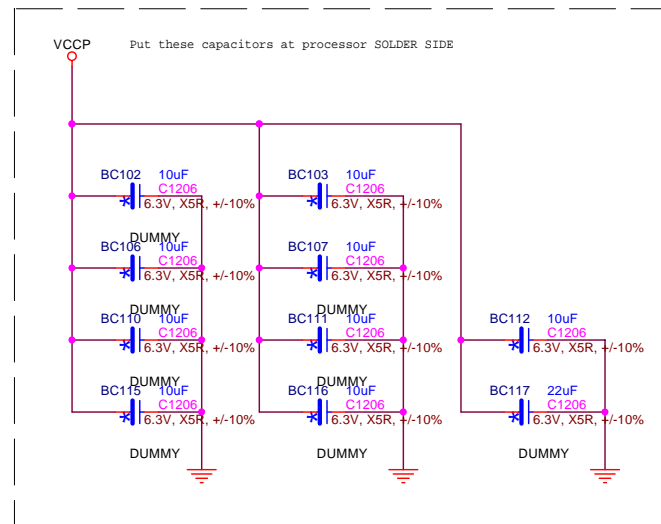
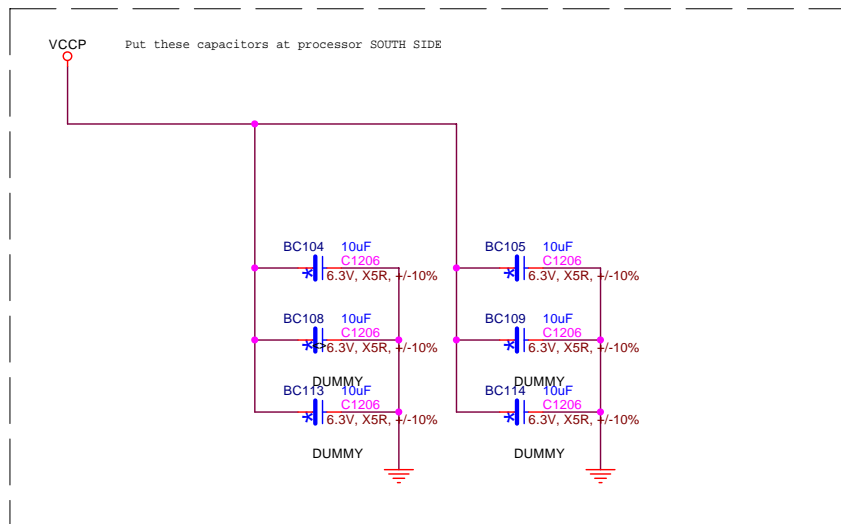
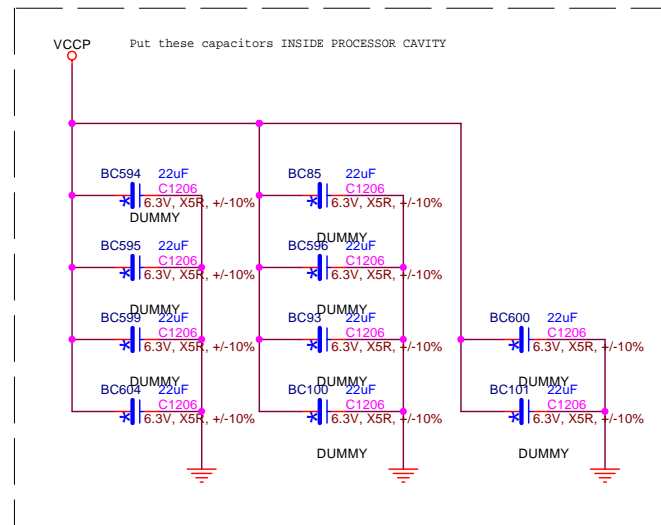
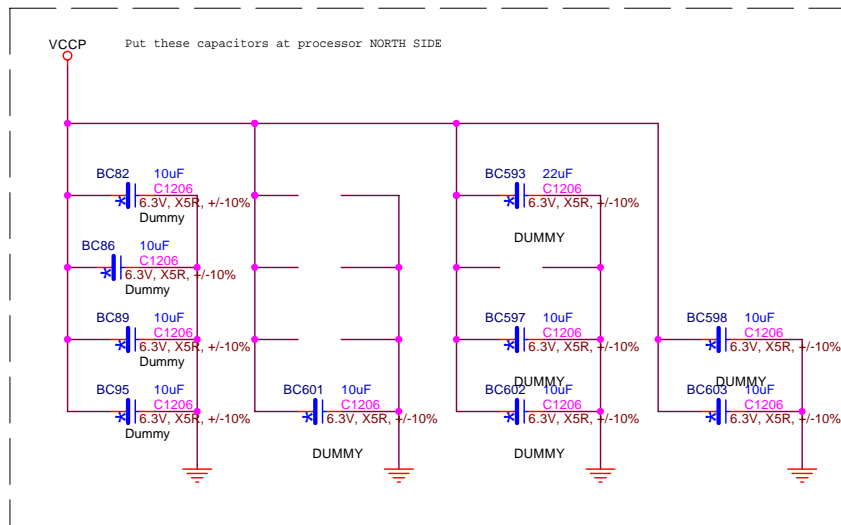
	R6	R7
optimized	51_1%	OPEN
compat#	OPEN	0 ohms

"CPU_optimized"
can be delete

FOXCONN
FOXCONN PCEG

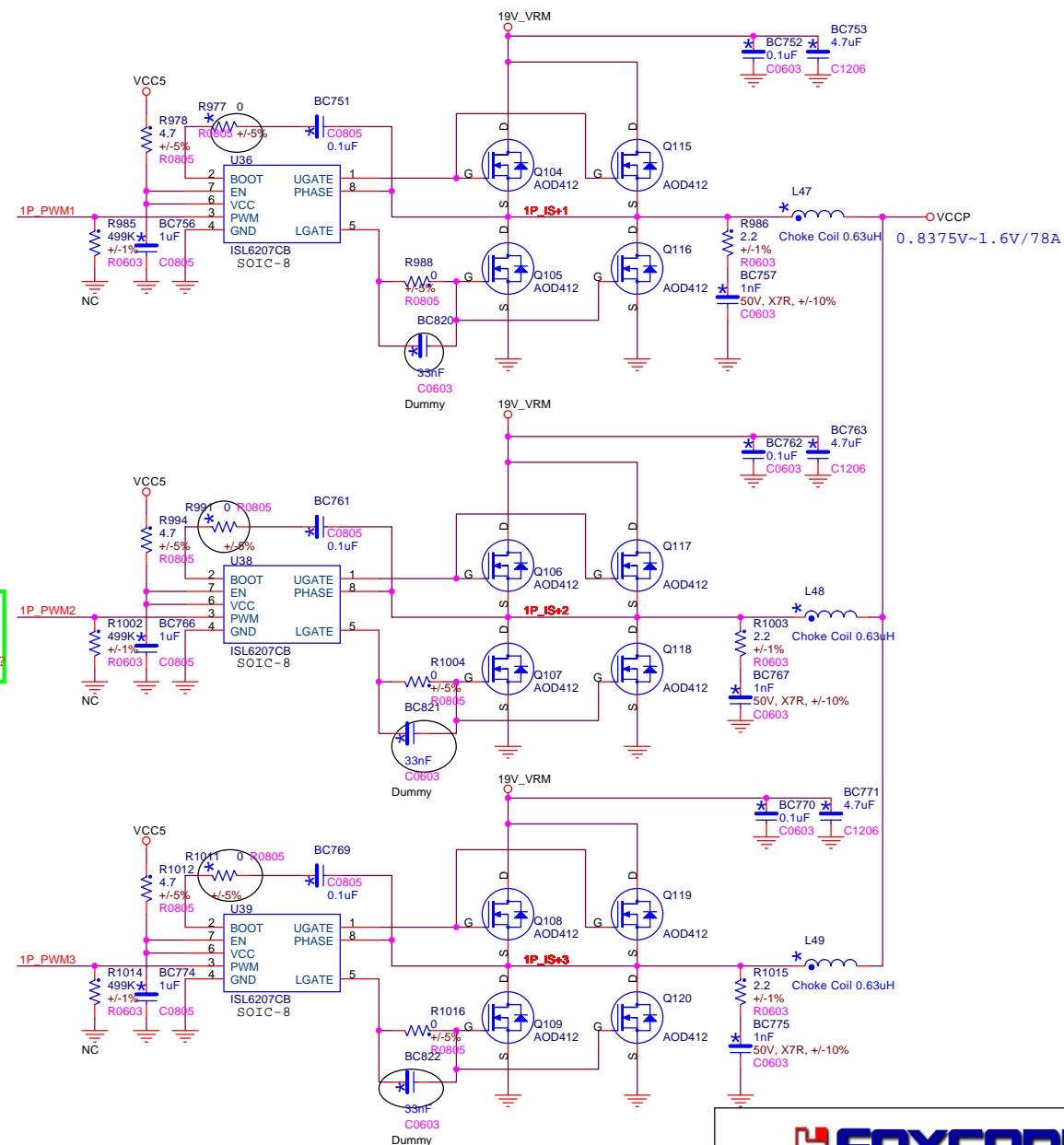
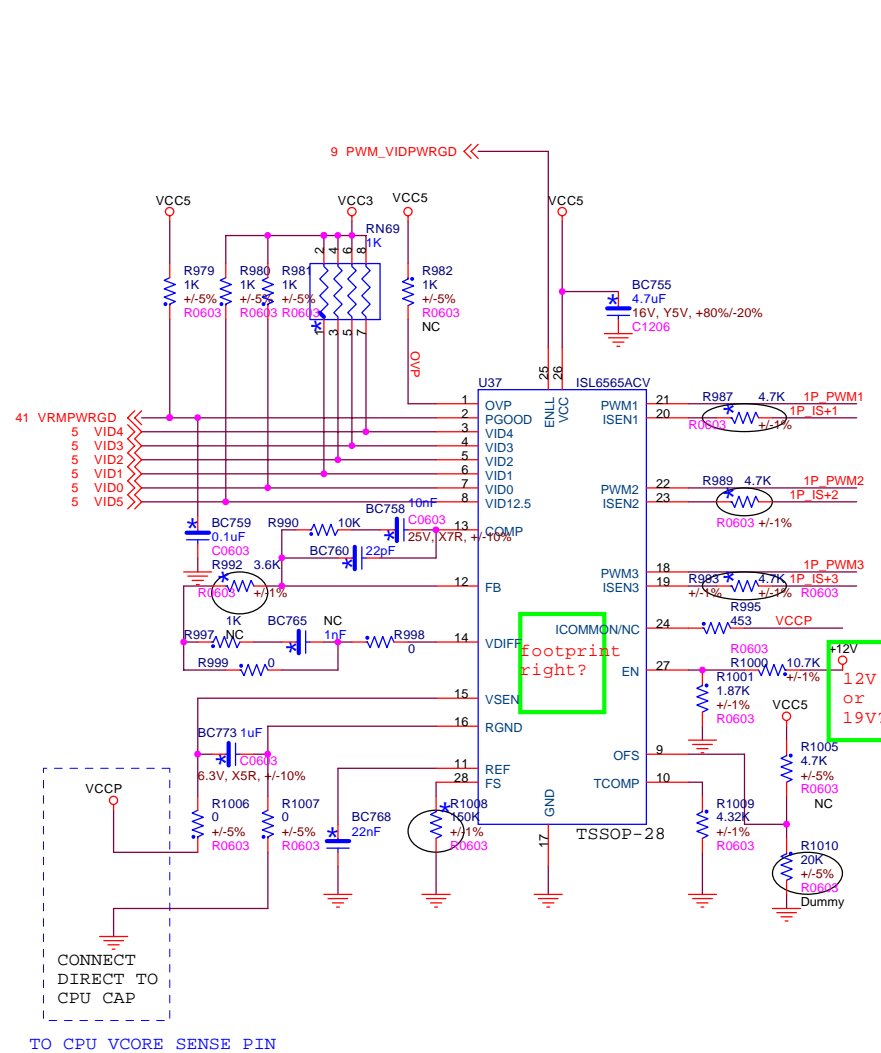
Title NORTHWOOD/PRESCOTT-1

Size Document Number 661S01
Date: Wednesday, September 22, 2004 Sheet 5 of 43



P.S. Choose X7R/X5R components instead of Y5V for all 10uF_1206 capacitors on this page.

ISL6565ACV FOR Intel P4 VRD10.1 POWER CKT



FOXCONN PCEG

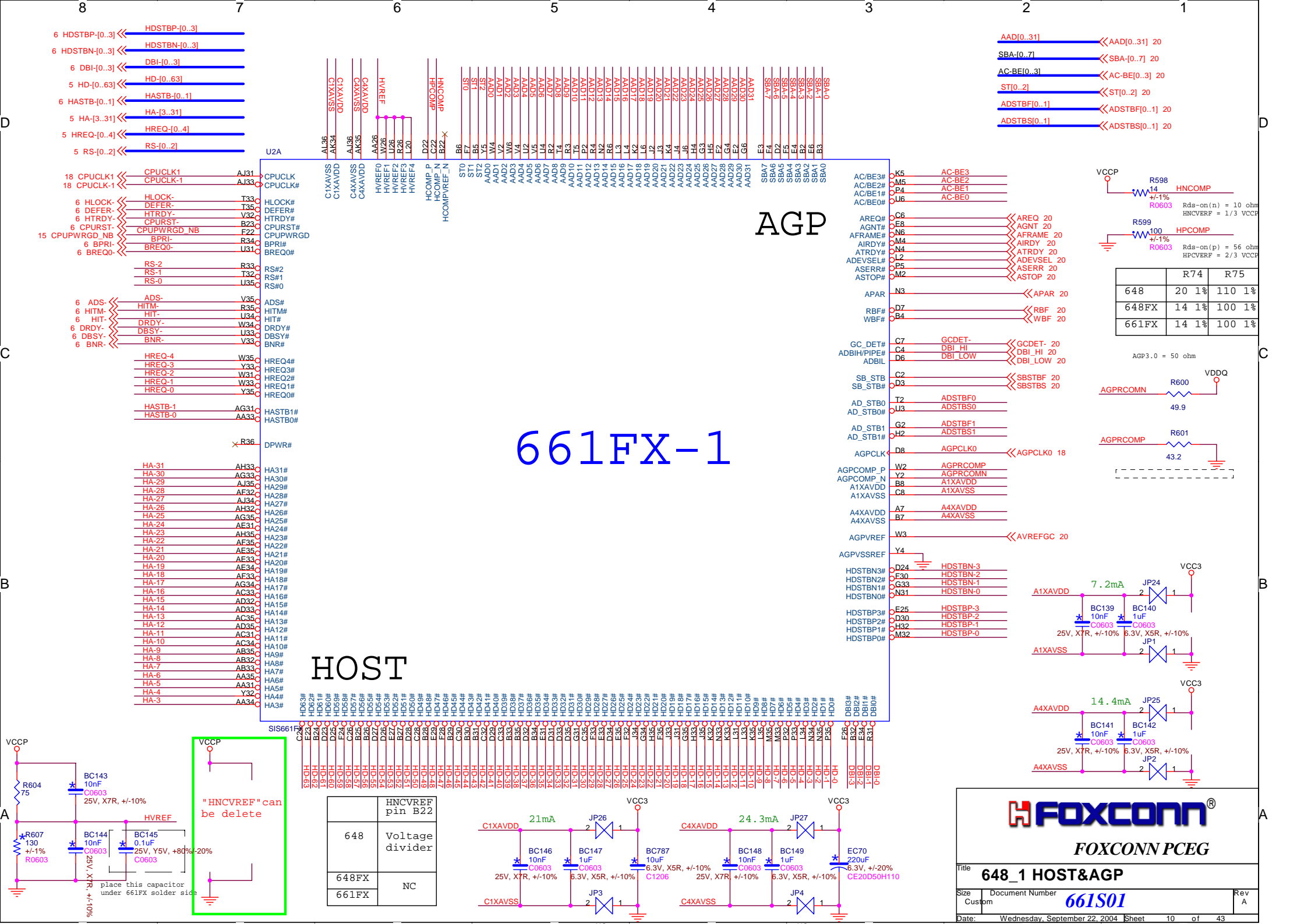
Title	648 1 VCCP
-------	------------

Size	Document Number
Custom	661S01

Date: Wednesday, September 22, 2004 Sheet 8 of 43

Rev
A

Re



/RMD[0..63] <</RMD[0..63] 22,24
/RDQM[0..7] <</RDQM[0..7] 22,24
/RDQS[0..7] <</RDQS[0..7] 22,24
/RMA[0..14] <</RMA[0..14] 22,24
/RCS[0..3] <</RCS[0..3] 22,24
CKE[0..3] <<CKE[0..3] 22

Rs place close to DIMM1

/RMD1 RN55 1 2 MD1
/RMD5 3 4 MD5
/RMD4 5 6 MD4
/RMD0 10 7 8 MD0
/RMD6 RN56 1 2 MD6
/RMD2 3 4 MD2
/RDQM0 5 6 DQM0
/RDQS0 10 7 8 DQS0
/RMD9 RN72 1 2 MD9
/RMD8 3 4 MD8
/RMD3 5 6 MD3
/RMD7 10 7 8 MD7
/RMD11 RN57 1 2 MD11
/RMD10 3 4 MD10
/RMD15 5 6 MD15
/RMD14 10 7 8 MD14
/RDQM1 RN58 1 2 DQM1
/RDQS1 3 4 DQS1
/RMD13 5 6 MD13
/RMD12 10 7 8 MD12
/RMD21 RN70 1 2 MD21
/RMD17 3 4 MD17
/RMD16 5 6 MD16
/RMD20 10 7 8 MD20

/RMD22 RN74 1 2 MD22
/RMD18 3 4 MD18
/RDQM2 5 6 DQM2
/RDQS2 10 7 8 DQS2
/RMD25 RN59 1 2 MD25
/RMD24 3 4 MD24
/RMD19 5 6 MD19
/RMD23 10 7 8 MD23
/RMD31 RN59 1 2 MD31
/RMD27 3 4 MD27
/RMD30 5 6 MD30
/RMD26 10 7 8 MD26
/RDQM3 RN60 1 2 DQM3
/RDQS3 3 4 DQS3
/RMD25 5 6 MD25
/RMD29 10 7 8 MD29
/RMD33 RN61 1 2 MD33
/RMD37 3 4 MD37
/RMD36 5 6 MD36
/RMD32 10 7 8 MD32
/RMD38 RN62 1 2 MD38
/RDQM4 3 4 DQM4
/RMD34 5 6 MD34
/RDQS4 10 7 8 DQS4
/RMD44 RN10 1 2 MD44
/RMD40 3 4 MD40
/RMD35 5 6 MD35
/RMD39 10 7 8 MD39

/RDQS5 RN11 1 2 DQS5
/RDQM5 3 4 DQM5
/RMD41 5 6 MD41
/RMD45 10 7 8 MD45
/RMD47 RN11 1 2 MD47
/RMD43 3 4 MD43
/RMD46 5 6 MD46
/RMD42 10 7 8 MD42
/RMD50 RN12 1 2 MD50
/RDQS6 3 4 DQS6
/RMD54 5 6 MD54
/RDQM6 10 7 8 DQM6
/RMD53 RN13 1 2 MD53
/RMD52 3 4 MD52
/RMD49 5 6 MD49
/RMD48 10 7 8 MD48
/RMD56 RN14 1 2 MD56
/RMD60 3 4 MD60
/RMD51 5 6 MD51
/RMD55 10 7 8 MD55
/RMD62 RN15 1 2 MD62
/RDQM7 3 4 DQM7
/RMD57 5 6 MD57
/RMD61 10 7 8 MD61
/RMD63 3 4 MD63
/RMD59 5 6 MD59
/RMD58 RN16 5 6 MD58
/RDQS7 10 7 8 DQS7

U2B

MD0 AN35
MD1 AP36
MD2 AK33
MD3 AM33
MD4 AN34
MD5 AK32
MD6 AR34
MD7 AN33
DQM0 AR36
DQS0 AP34
MD8 AM32
MD9 AL31
MD10 AR31
MD11 AL30
MD12 AN32
MD13 AR33
MD14 AN31
MD15 AM31
DQM1 AR32
DQS1 AP32
MD16 AP30
MD17 AR30
MD18 AM29
MD19 AL27
MD20 AN30
MD21 AN29
MD22 AL28
MD23 AN28
DQM2 AL29
DQS2 AP28
MD24 AP26
MD25 AN25
MD26 AR24
MD27 AL24
MD28 AL25
MD29 AR26
MD30 AM25
DQM3 AN24
DQS3 AP24
MD31 AR25
MD32 AN21
MD33 AP20
MD34 AN20
MD35 AL18
MD36 AM21
MD37 AR21
MD38 AL19
MD39 AM19
DQM4 AL20
DQS4 AR20
MD40 AL15
MD41 AL14
MD42 AN15
MD43 AR15
MD44 AL16
MD45 AM15
MD46 AN14
MD47 AL13
DQM5 AP16
DQS5/CSB5# DQM5
MD48 AM13
MD49 AL12
MD50 AL11
MD51 AR12
MD52 AP14
MD53 AR14
MD54 AN13
MD55 AP12
DQM6 AN12
DQS6 AR13
MD56 AL10
MD57 AR11
MD58 AM9
MD59 AR8
MD60 AM11
MD61 AN11
MD62 AP10
MD63 AN9
DQM7 AN10
DQS7/CSB7# DQS7

SIS661FX

Rs place close to DIMM1

MA0 AR23 /RMA0
MA1 AN23 /RMA1
MA2 AN22 /RMA2
MA3 AM23 /RMA3
MA4 AL23 /RMA4
MA5 AL26 /RMA5
MA6 AN26 /RMA6
MA7 AR27 /RMA7
MA8 AR28 /RMA8
MA9 AP22 /RMA9
MA10 AN18 /RMA10
MA11 AR22 /RMA11
MA12 AP28 /RMA12
MA13 AR27 /RMA13
MA14 AT14 /RMA14
NC

SRAS# AL17 /RSRAS- <</RSRAS- 22,24
SCAS# AR19 /RSCAS- <</RSCAS- 22,24
SWR# AN19 /RSWE- <</RSWE- 22,24

MD24 /RCS-0
CS0# AL16 /RCS-1
CS1# MD27 /RCS-2
CS2# AR17 /RCS-3
CS3# AP18
CS4# AR18
CS5#

AP4 CKE0
AT3 CKE1
AR3 CKE2
AP3 CKE3
AR2 CKE4
AN4 CKE5
AP2 S3AUXSW- <<S3AUXSW- 40

FWSDCLK0 AL21 R100 0 FWSDCLK0 <<FWSDCLK0 19

DRAMTEST AL22 <<BC154 10pF NC

DLLAVDD AL35 DLLAVDD

DLLAVSS AL34 DLLAVSS

DDRAVDD AM35 DDRAVDD

DDRAVSS AN36 DDRAVSS

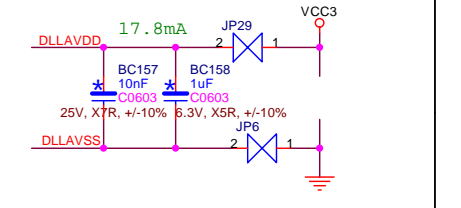
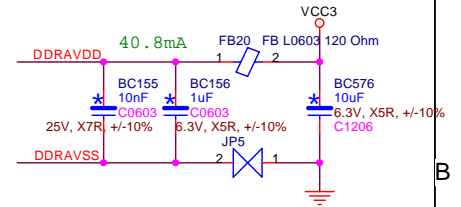
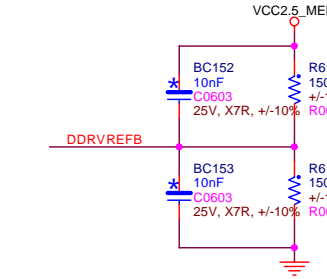
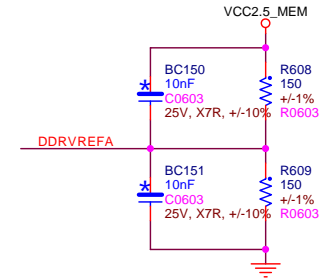
DDRREFB AF16 DDRREFB

DDRREFB AF23 DDRREFB

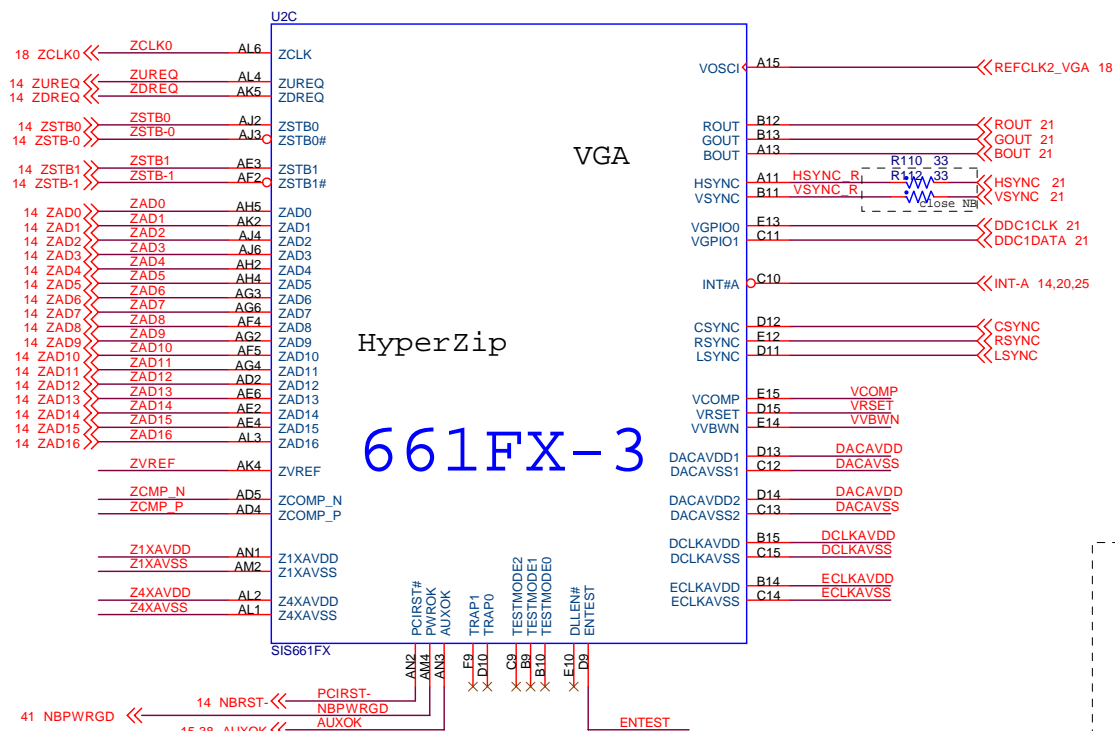
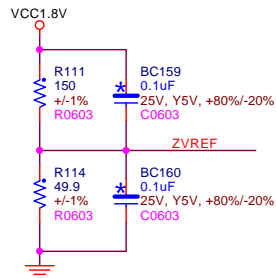
TRAP2 AP1 <<

DDRCOMP_P AR8 DDRCOMP

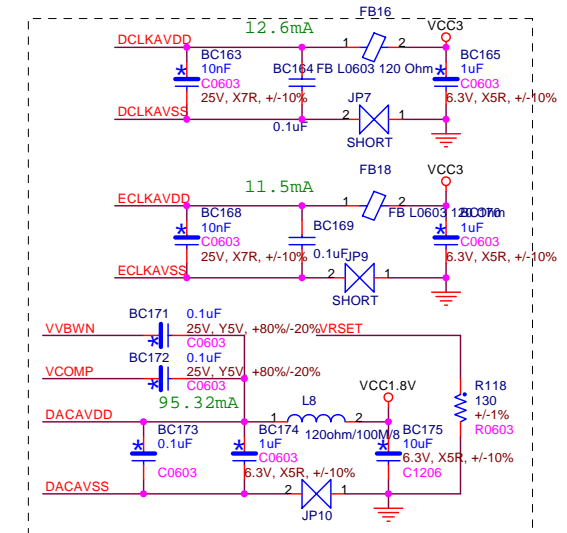
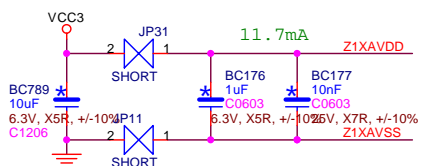
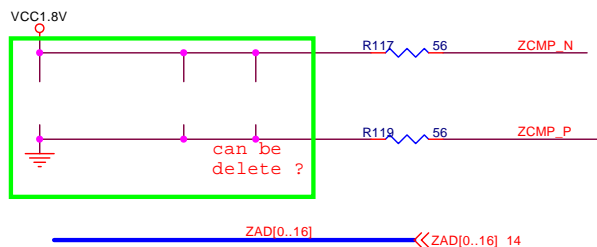
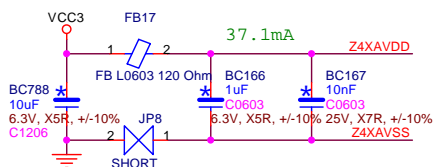
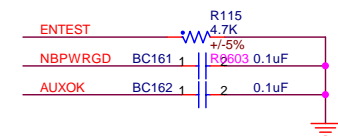
DDRCOMP_N AP8 DDRCOMP



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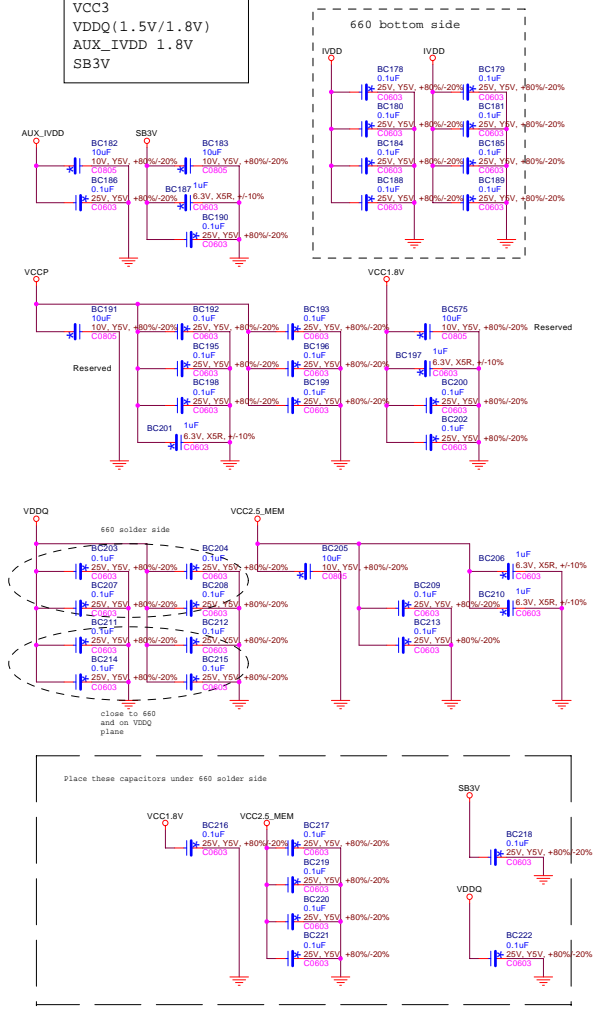
		Enable	Disable
RSYNC	VGA	1	0
LSYNC	panel link	1	0
CSYNC	VB	1	0



661FX-4

Power

IVDD 1.8V
VCC1.8V
VCCP
VCC2.5_MEM
VCC3
VDDQ(1.5V/1.8V)
AUX_IVDD 1.8V
SB3V

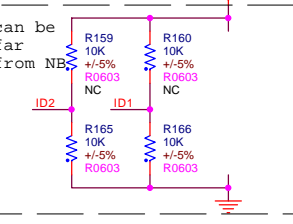
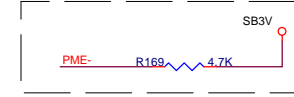
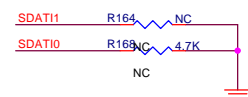
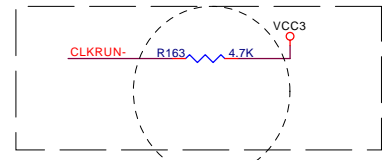
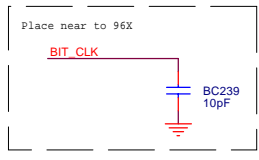
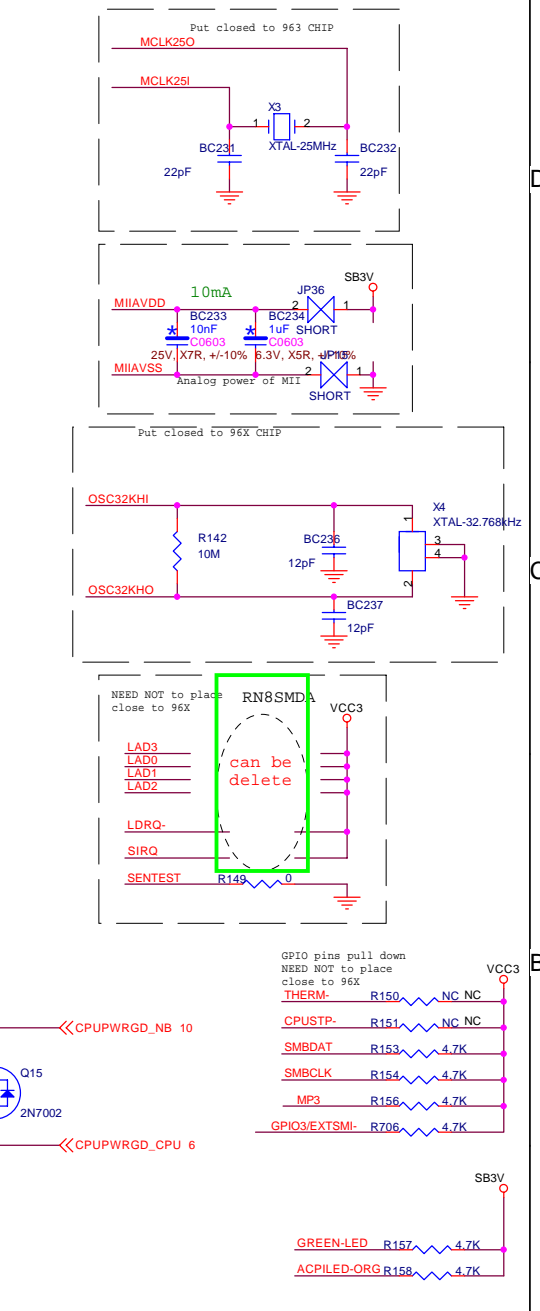
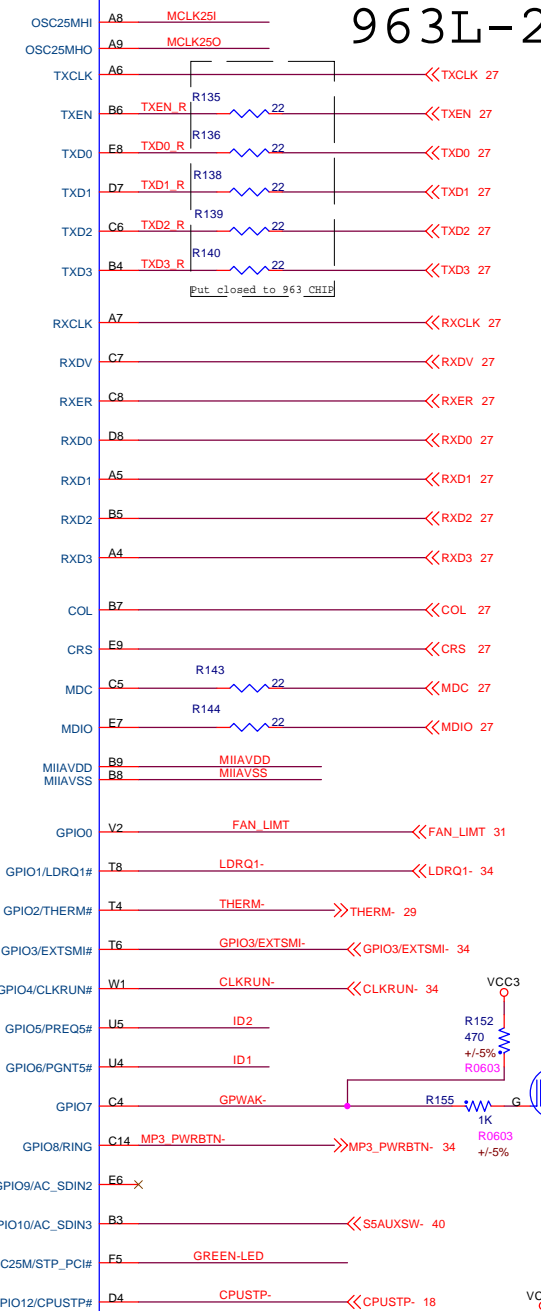
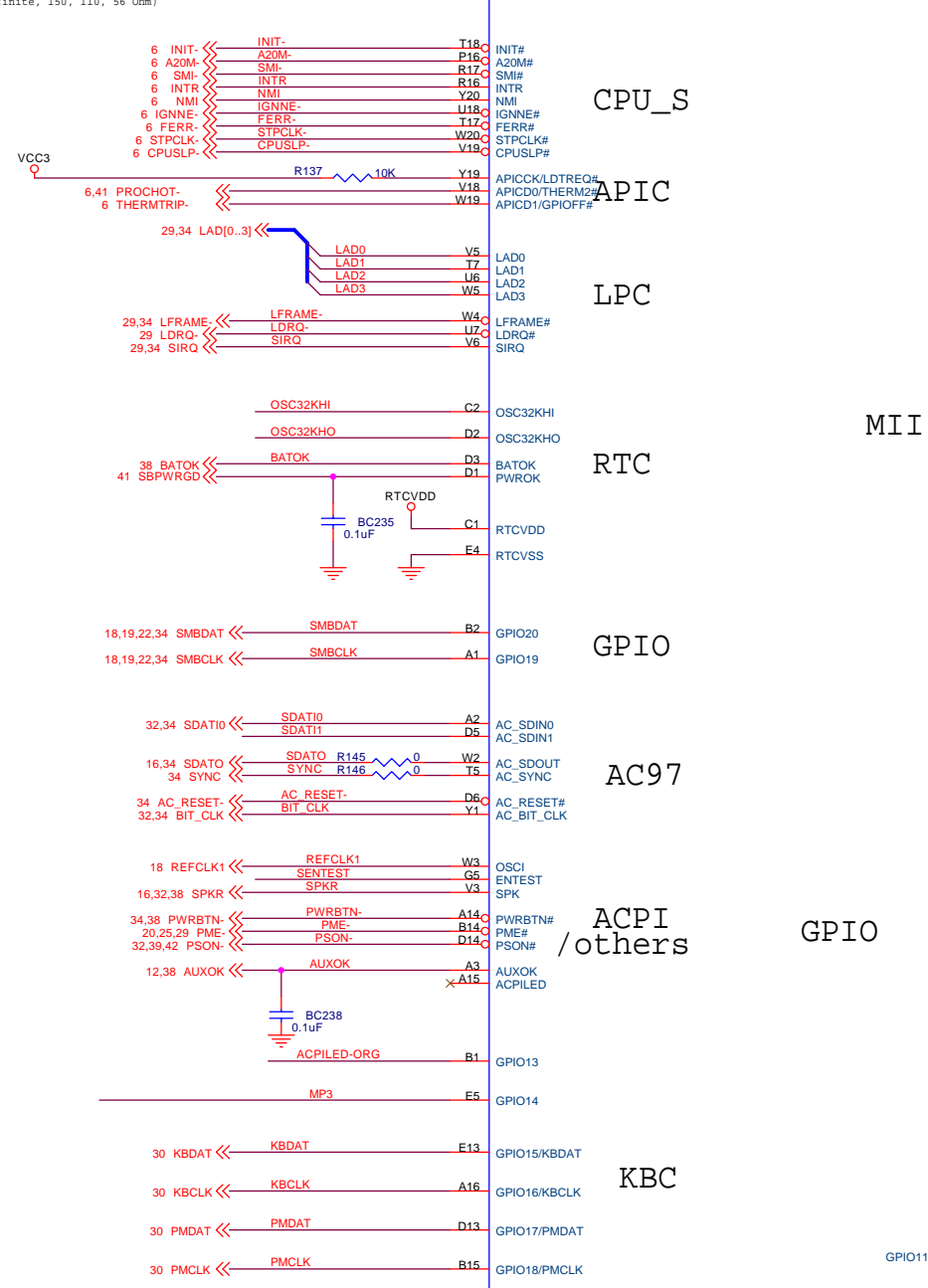


D

C

B

A



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FOXCONN PCEG

Title: **963-2 LPC/MI I/CPU/GPIO**

Size: Custom, Document Number: **661S01**, Rev: A

Date: Wednesday, September 22, 2004, Sheet 15 of 43

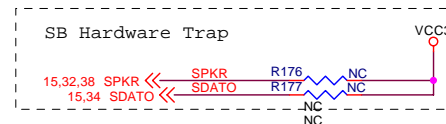
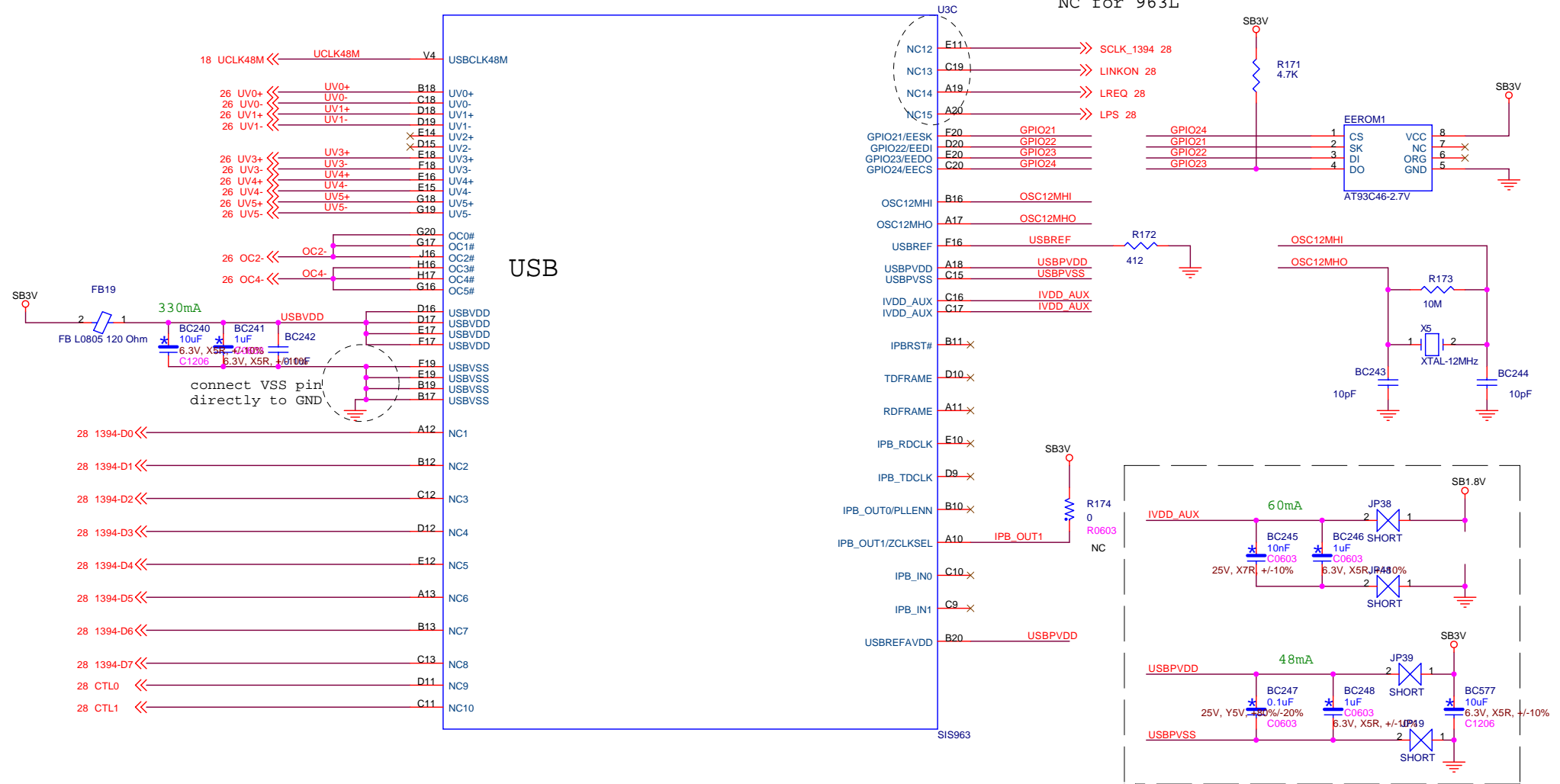
D

C

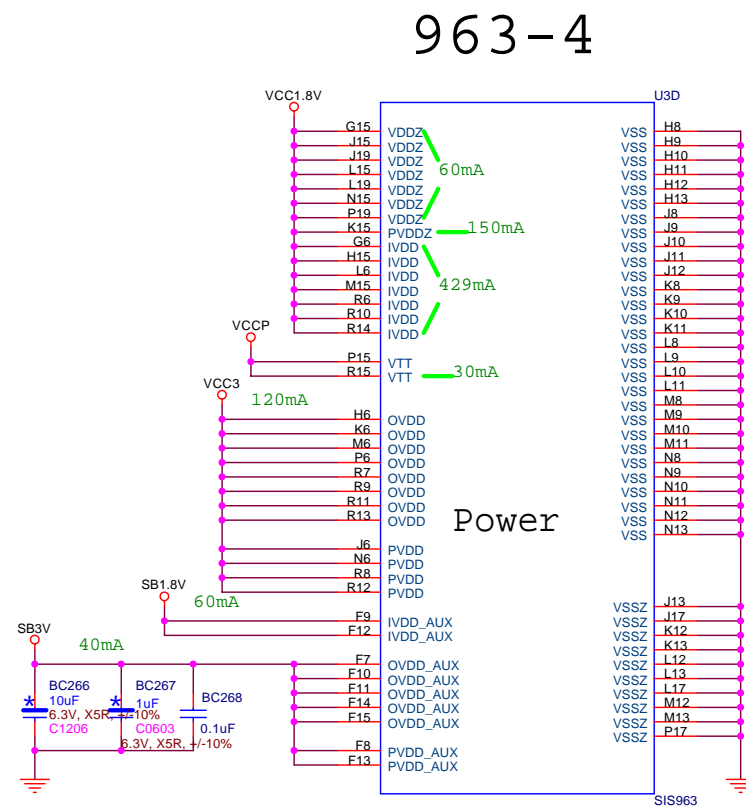
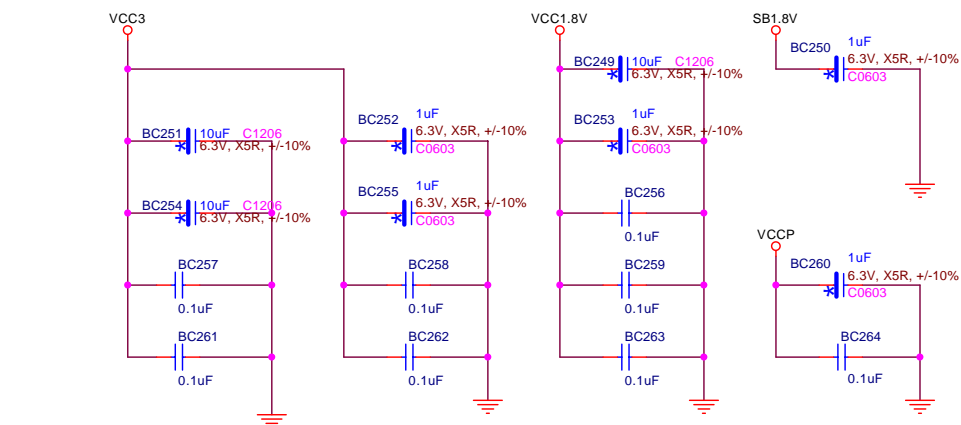
B

A

963-3



		Title	
		963-3 USB	
Size	Document Number	Rev	
Custom	661S01	A	
Date: Wednesday, September 22, 2004 Sheet 16 of 43			



Main Clock Generator

OPTIONS

Cypress: CY28381

ICS: ICS952011

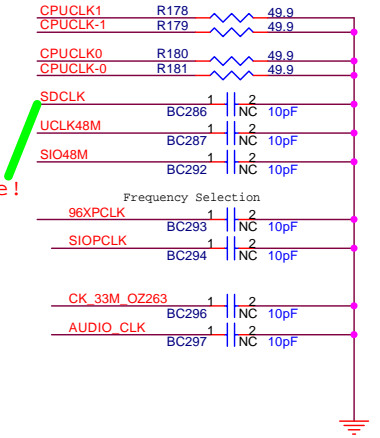
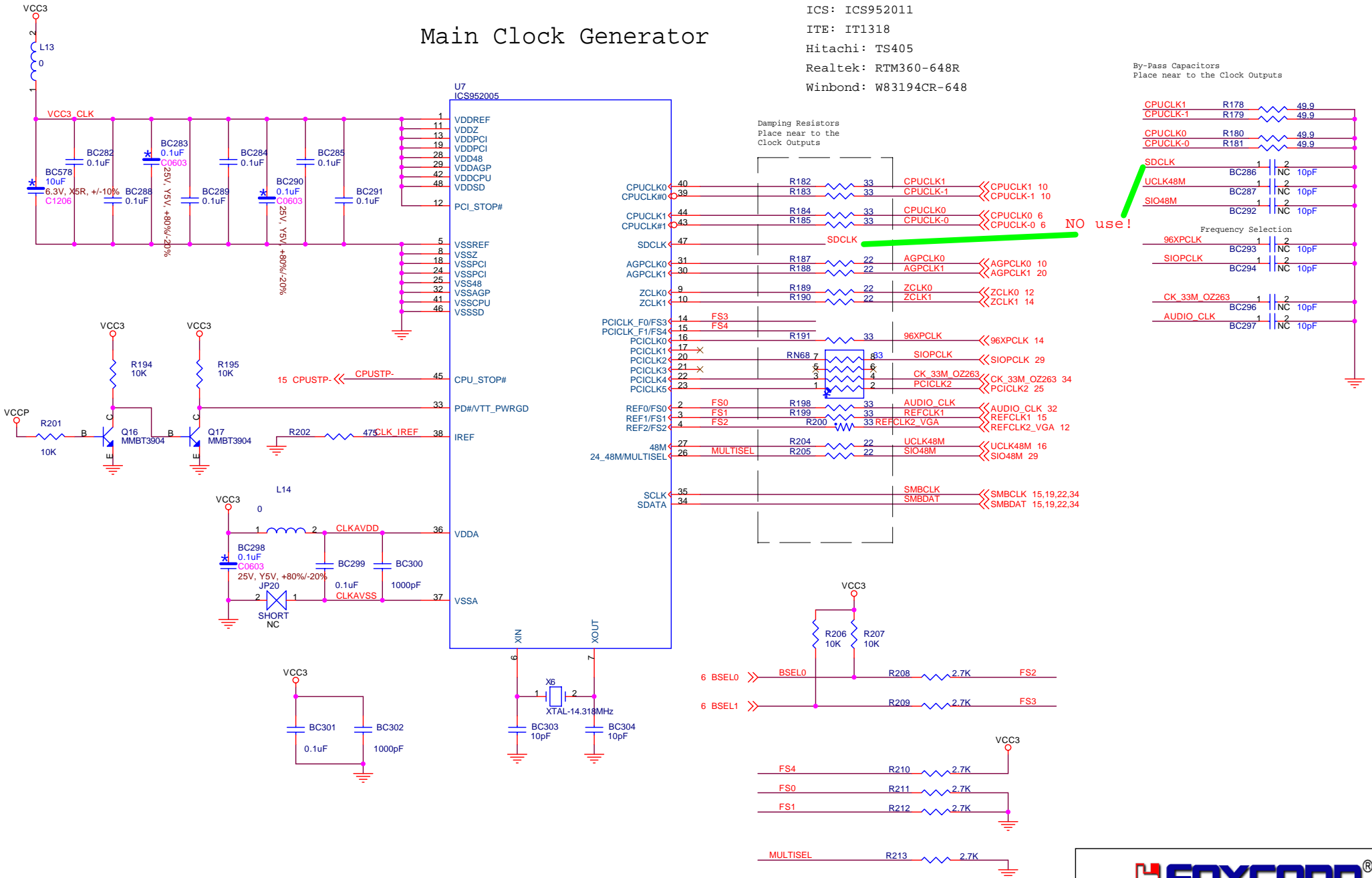
ITE: IT1318

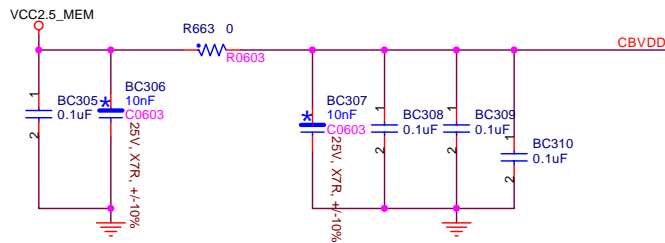
Hitachi: TS405

Realtek: RTM360-648R

Winbond: W83194CR-648

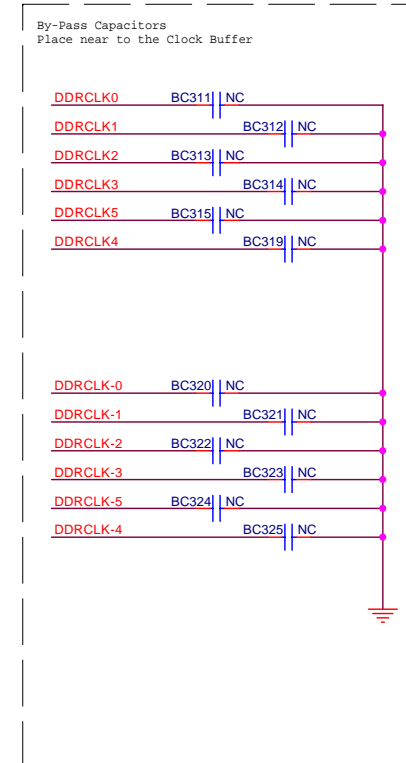
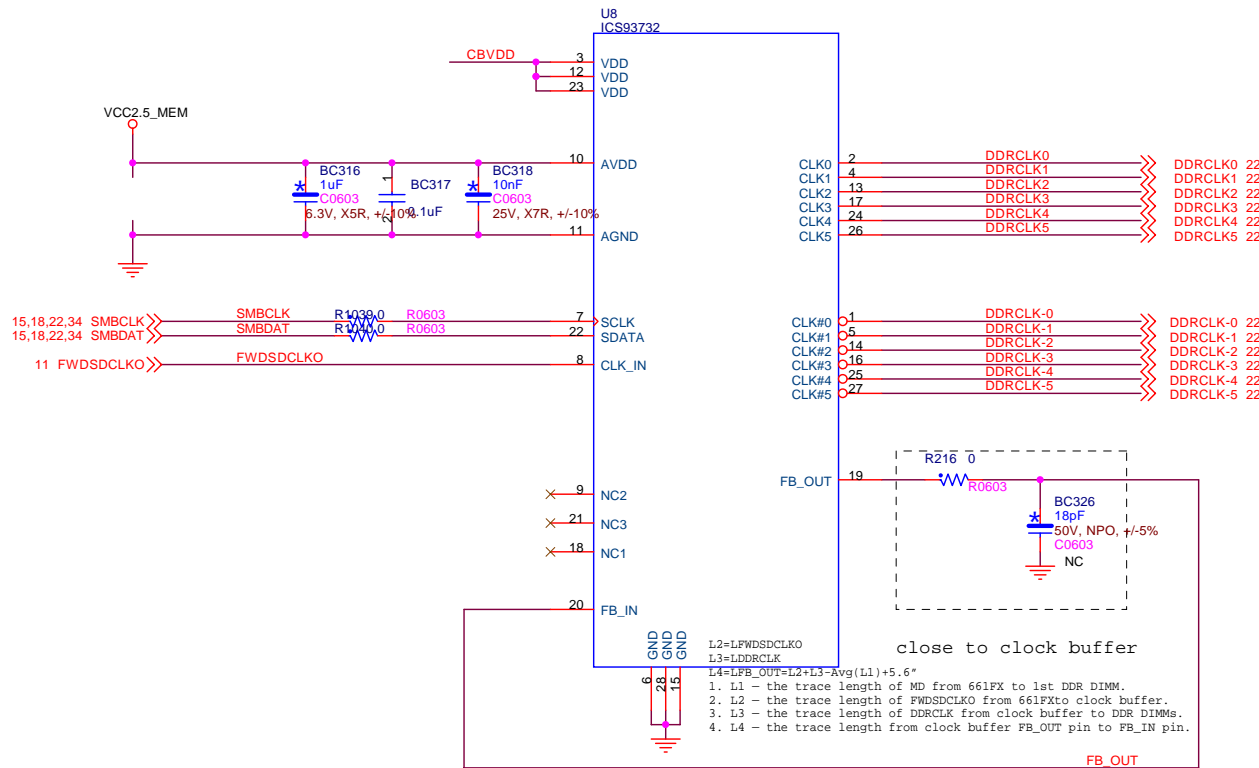
By-Pass Capacitors
Place near to the Clock Outputs





DDRCLK[0..5] 22
DDRCLK-[0..5] 22

Clock Buffer (DDR)

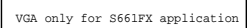


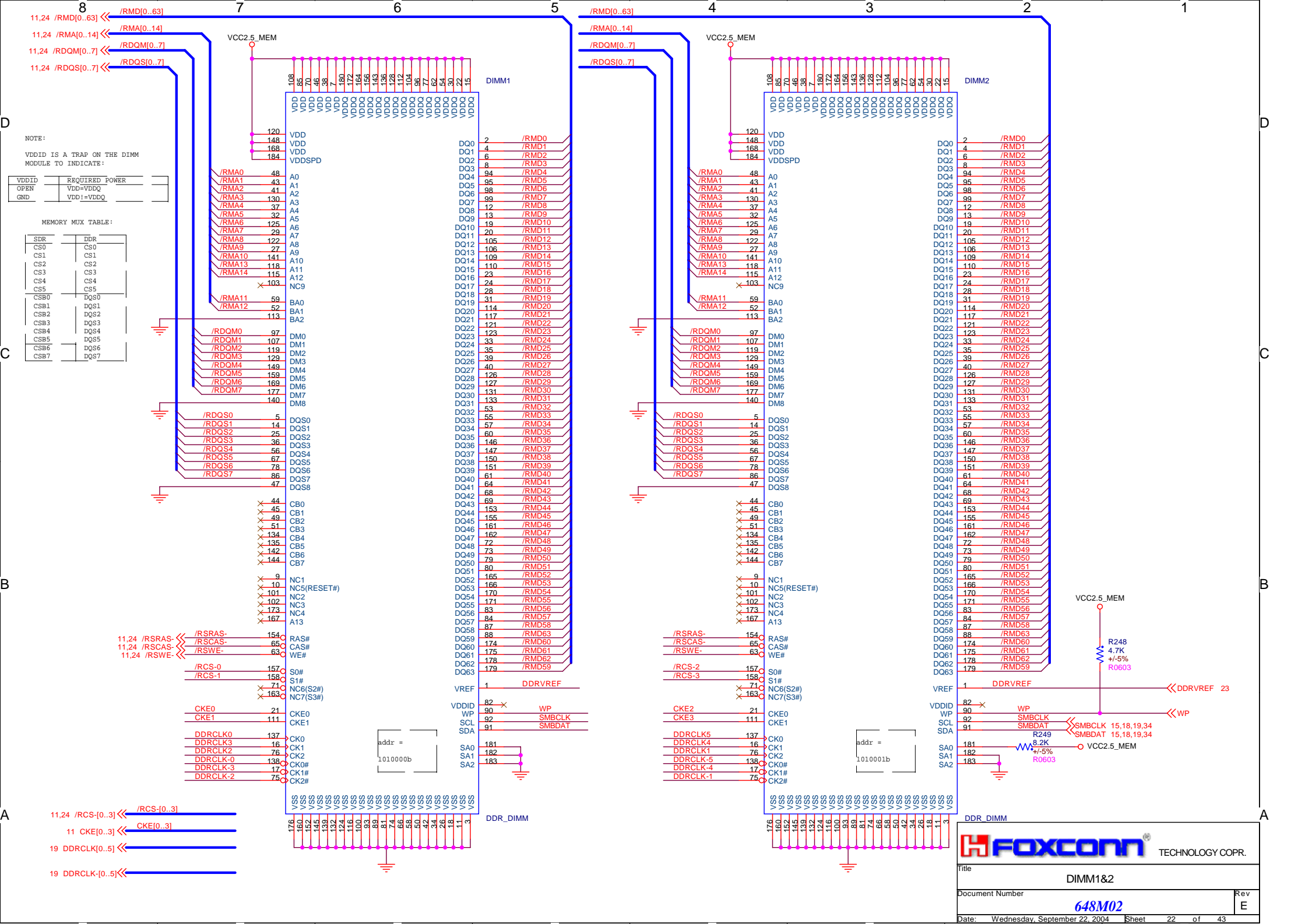
OPTIONS

DDR DIMMx2 ITE: IT1816
Hitachi: CDCV852(DDR333), CDCV854(DDR400)
Cypress: CY28352
Realtek: RTM680-627

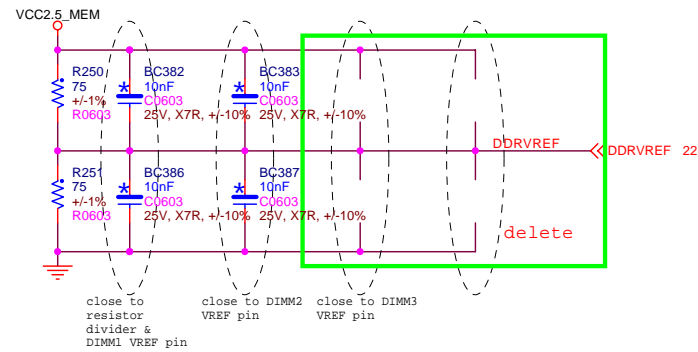
FOXCONN
FOXCONN PCEG

Title DDR CLOCK Buffer		
Size Custom	Document Number 648M02	Rev E
Date:	Wednesday, September 22, 2004	Sheet 19 of 43

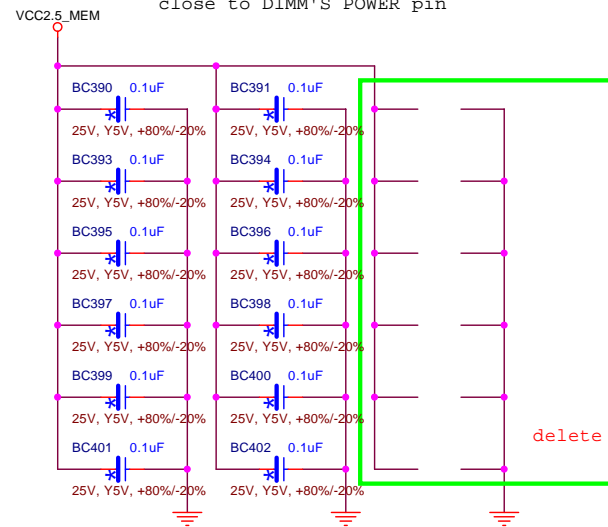




DDRVREF GEN. & DECOUPLING



DIMM BYPASS DECOUPLING close to DIMM'S POWER pin



FOXCONN PCEG

Title DIMM Power

Size Custom Document Number 648M02

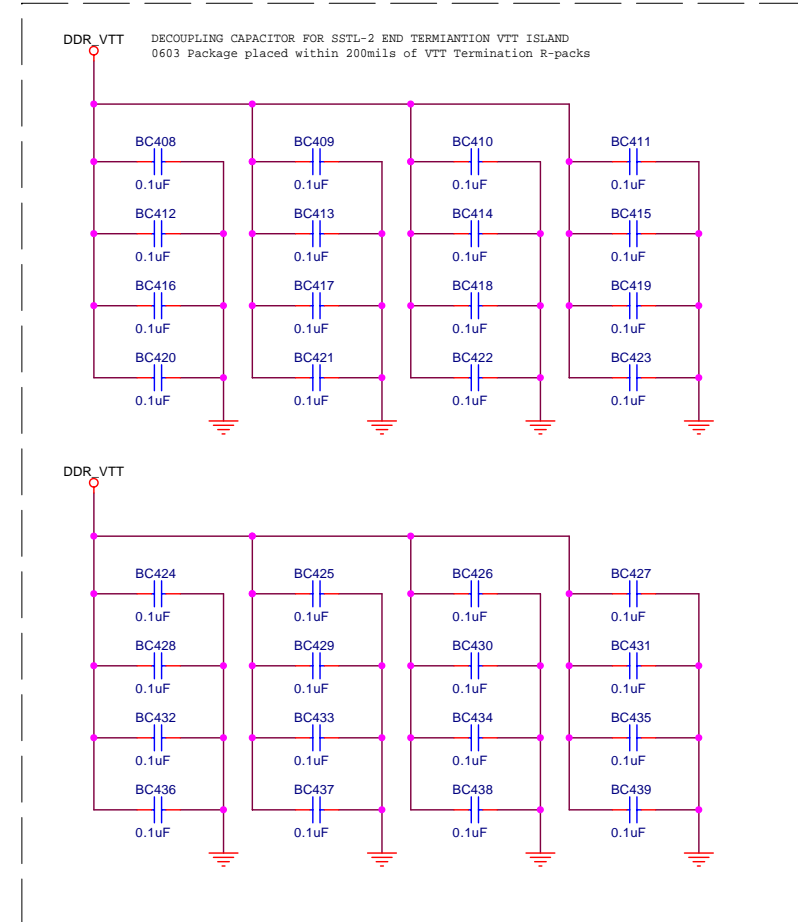
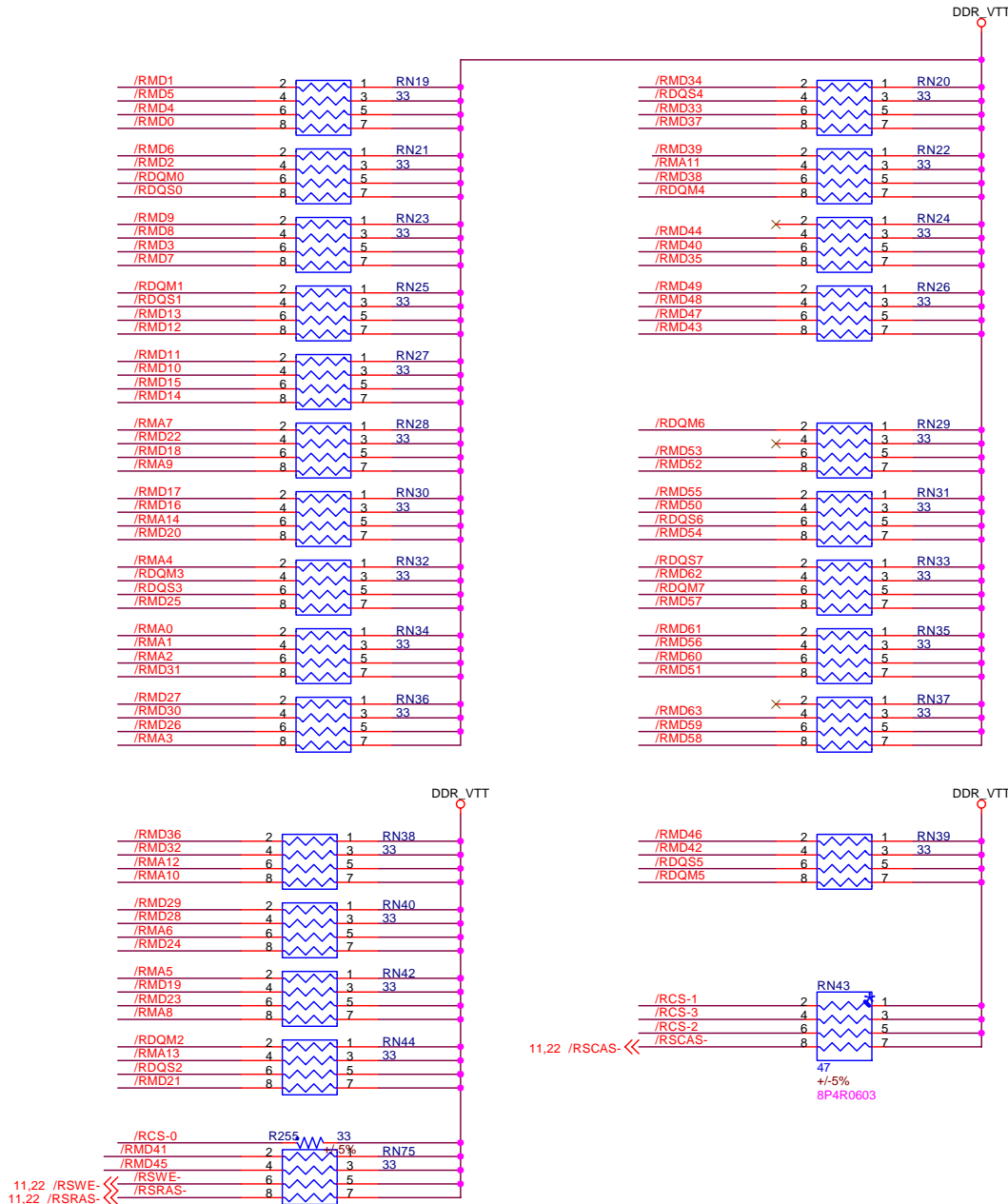
Rev E

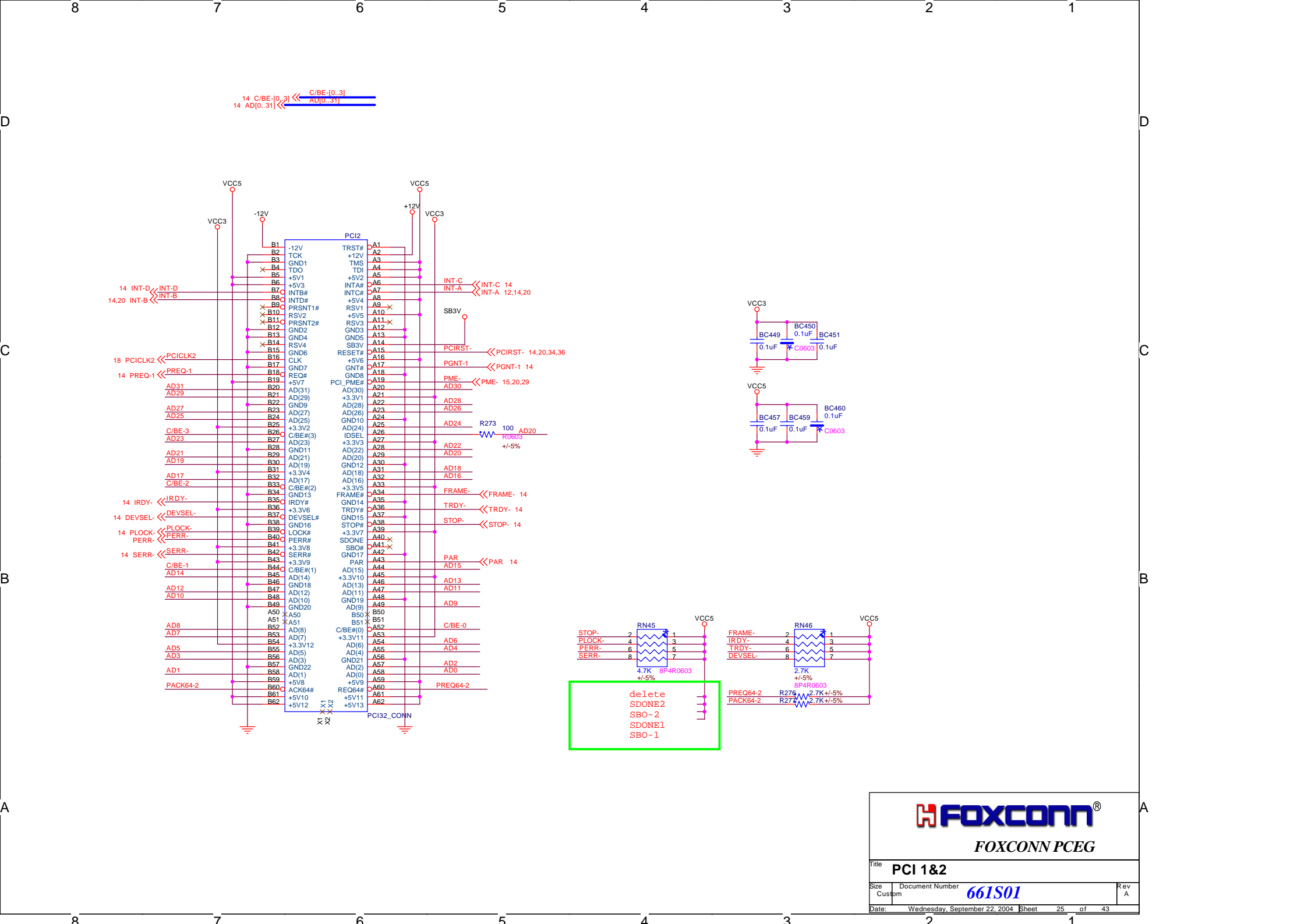
Date: Wednesday, September 22, 2004 Sheet 23 of 43

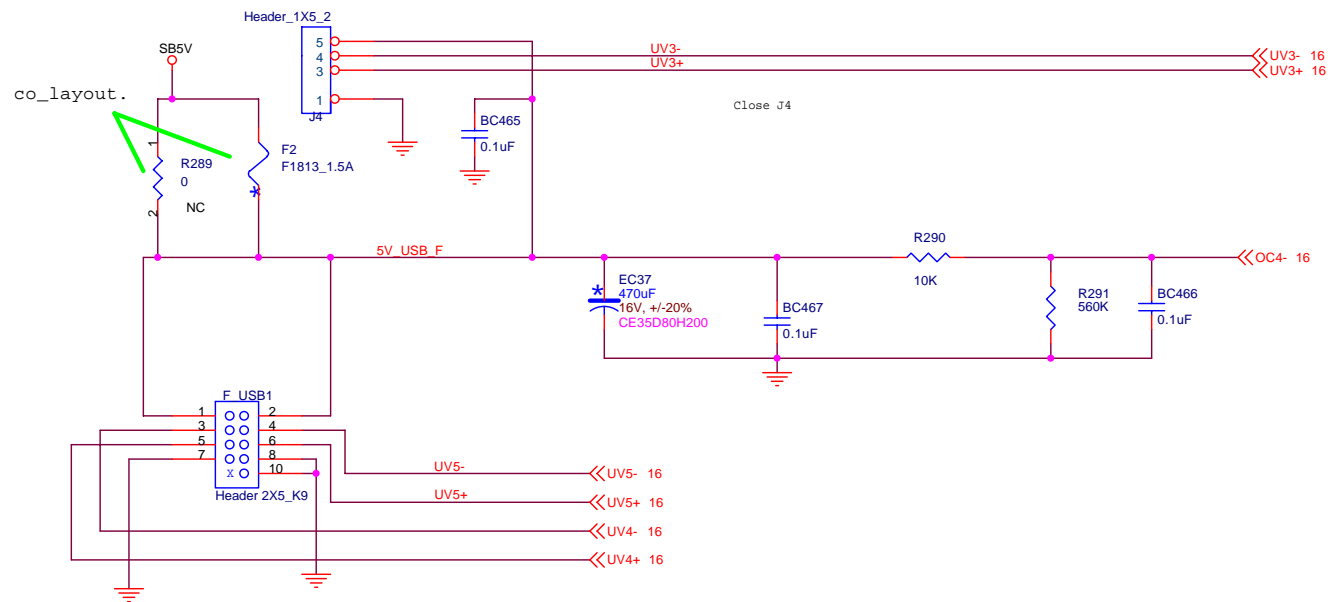
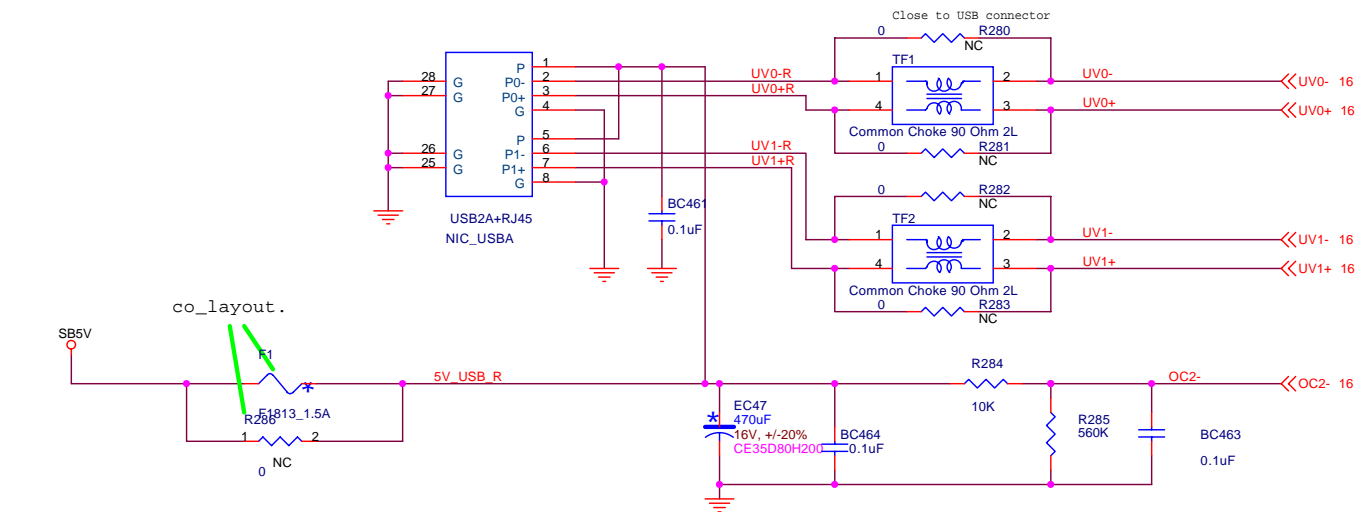
SSTL-2 Termination Resistors

/RMD[0..63] << /RMD[0..63] 11,22
 /RDQM[0..7] << /RDQM[0..7] 11,22
 /RDQS[0..7] << /RDQS[0..7] 11,22
 /RMA[0..14] << /RMA[0..14] 11,22
 /RCS[0..3] << /RCS[0..3] 11,22

	SDR		DDR		
MD/DQM (/DQS)	LV-CMOS	R _s	SSTL-2	R _s	R _{tt}
MA/Control	LV-CMOS	0/10/-	SSTL-2	10	33
CS	LV-CMOS	10	SSTL-2	0	33
VKE	DD 3.3V	0	SSTL-2	0	47

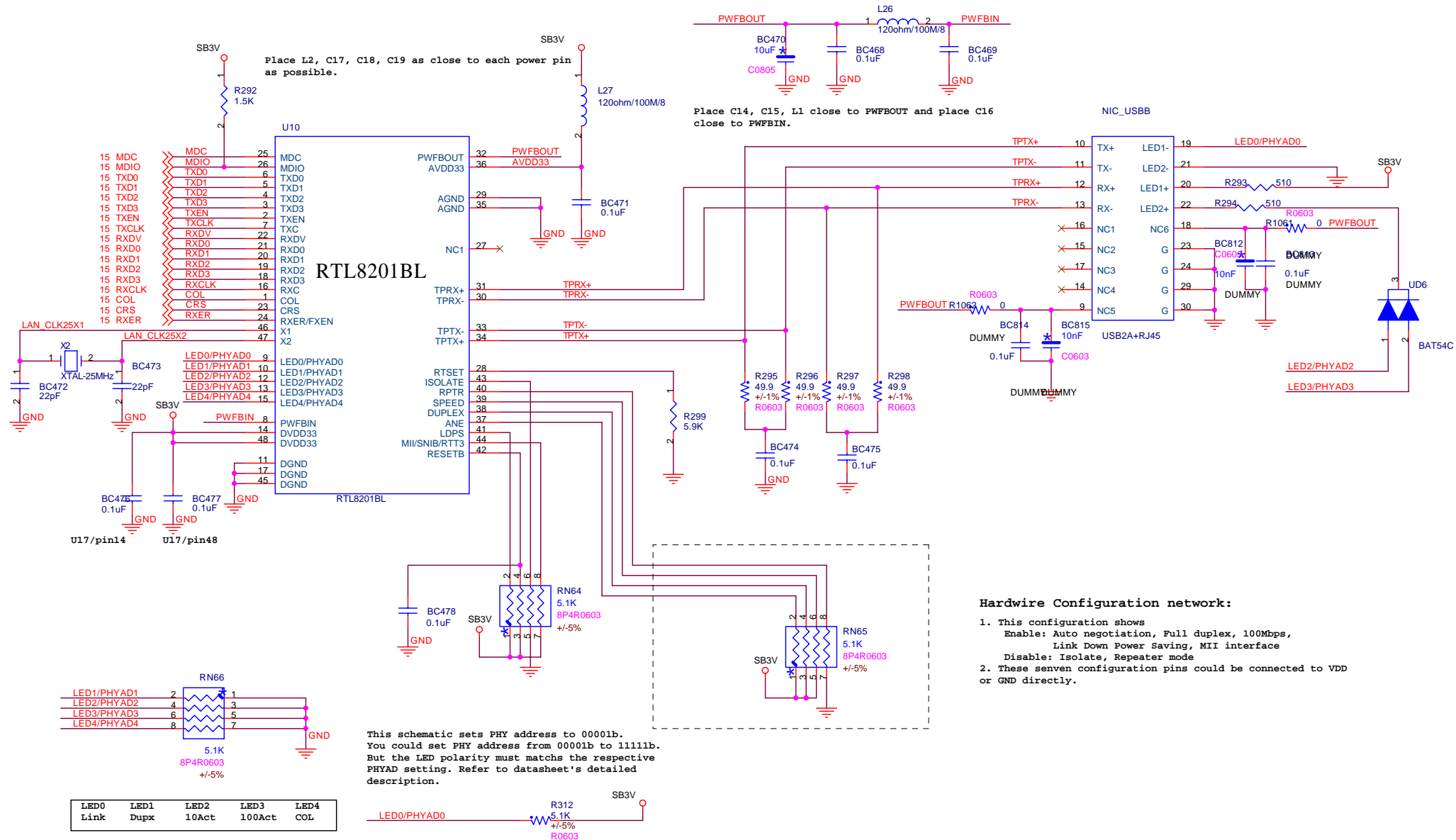






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Title	USB0,1,2,3		
Size	Custom	Document Number	661S01
Date:	Wednesday, September 22, 2004	Sheet	26 of 43
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Hardwire Configuration network:

1. This configuration shows
 Enable: Auto negotiation, Full duplex, 100Mbps,
 Link Down Power Saving, MII interface
 Disable: Isolate, Repeater mode
2. These seven configuration pins could be connected to VDD or GND directly.

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FOXCONN PCEG

Title **LAN PHY**

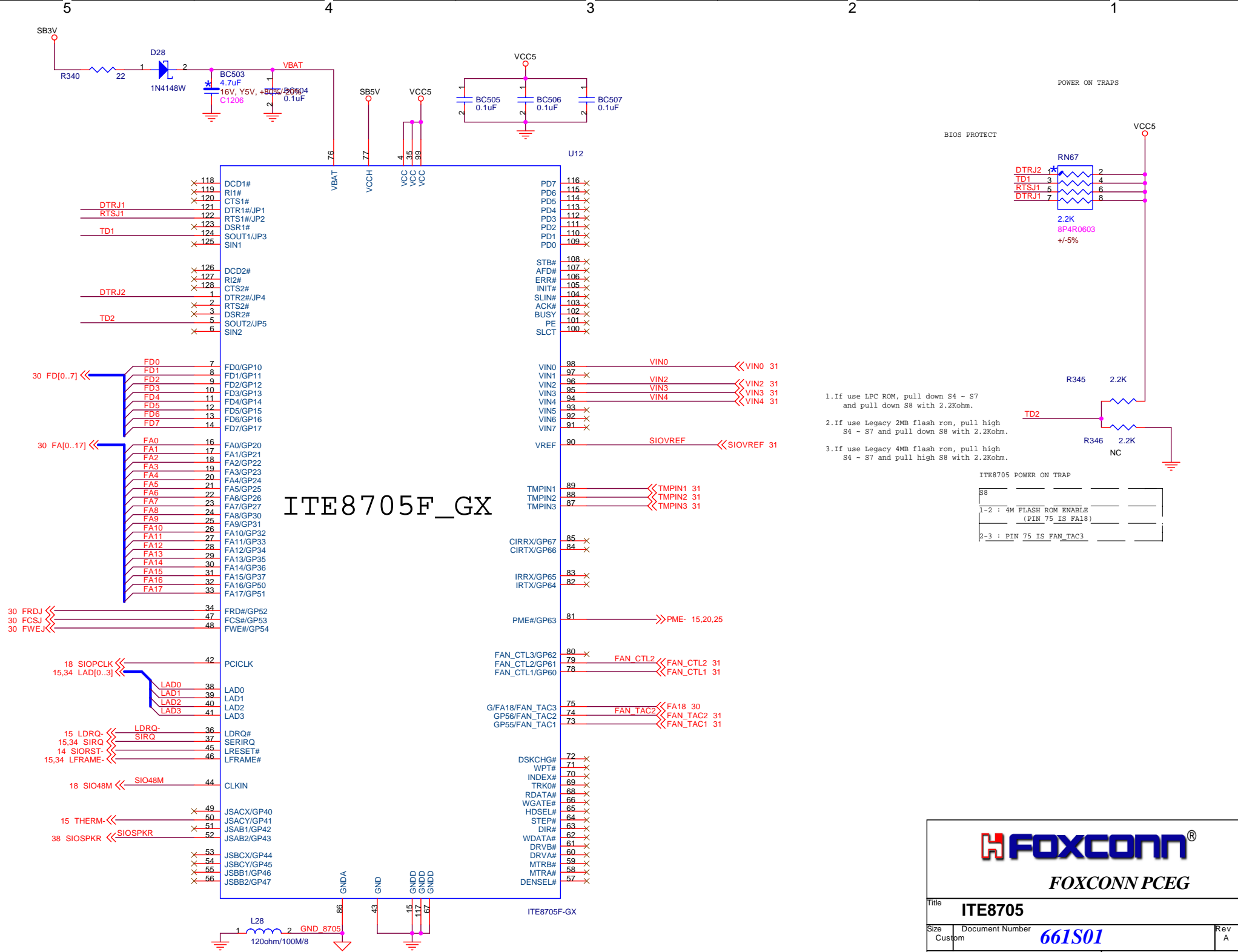
Size Custom Document Number **661S01**

Rev A

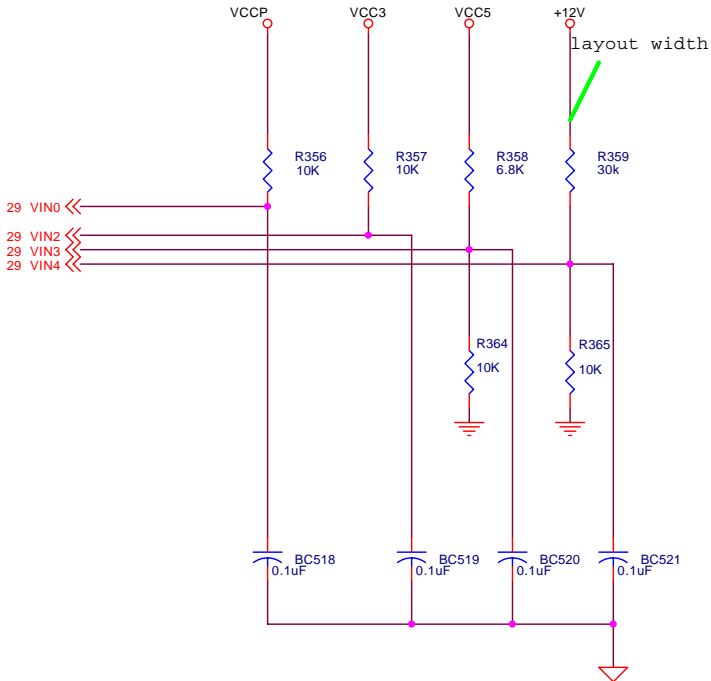
Date: Wednesday, September 22, 2004 Sheet 27 of 43



Date: Wednesday, September 22, 2004 Sheet 28 of 43

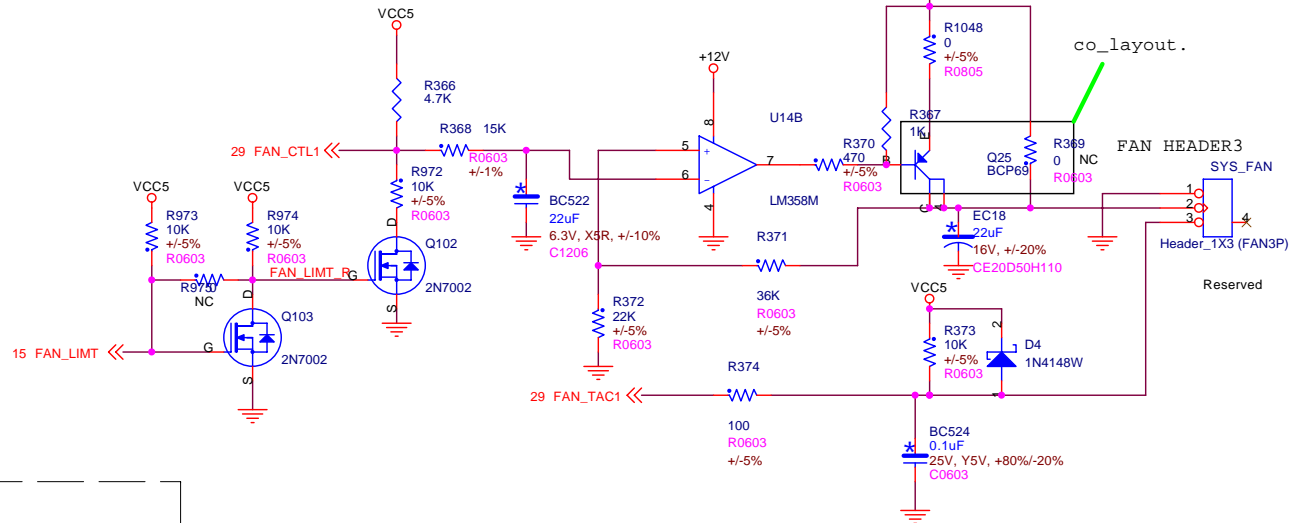
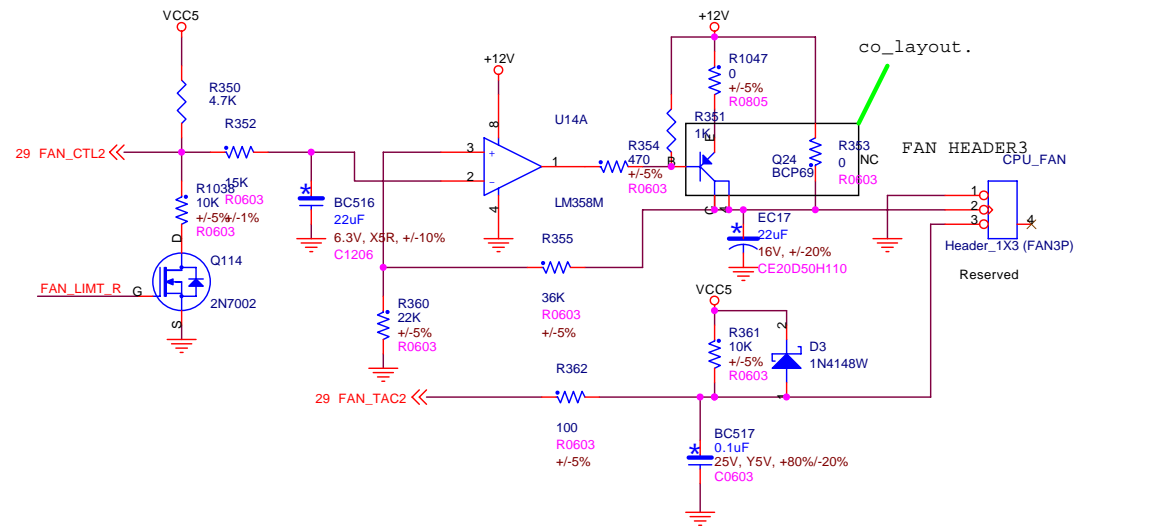
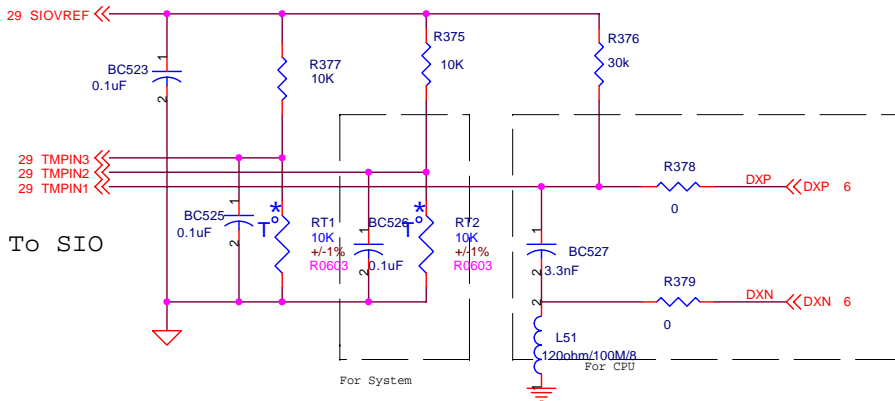


Voltage Monitor



Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode

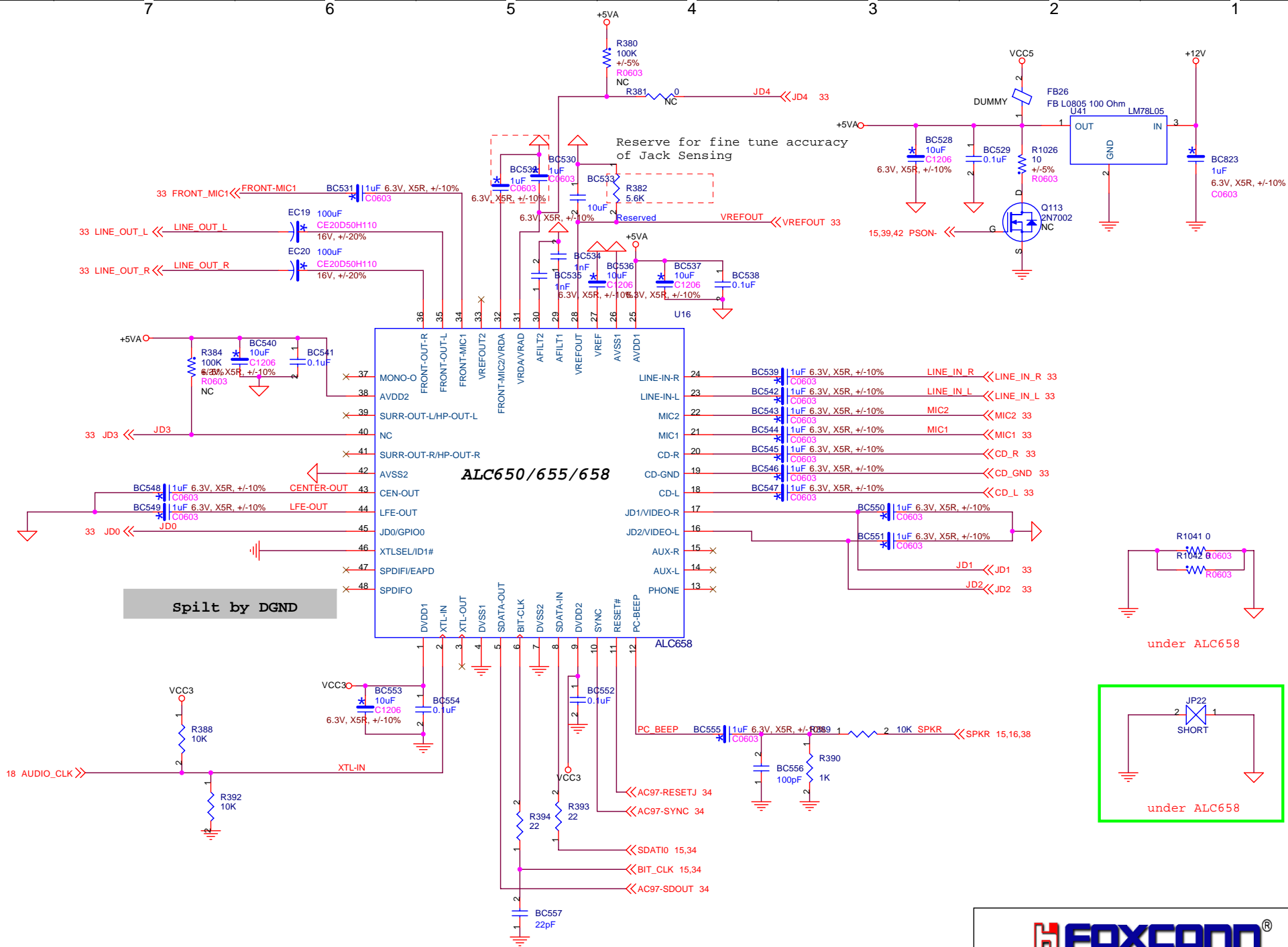


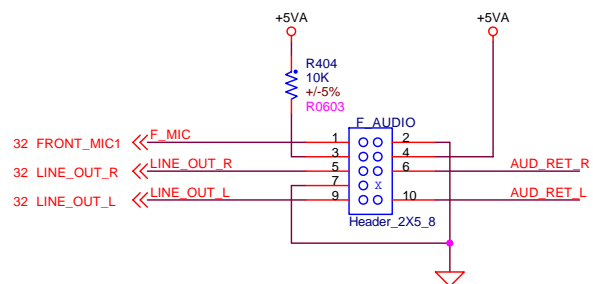
Title	FAN
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Size	Document Number	661S01
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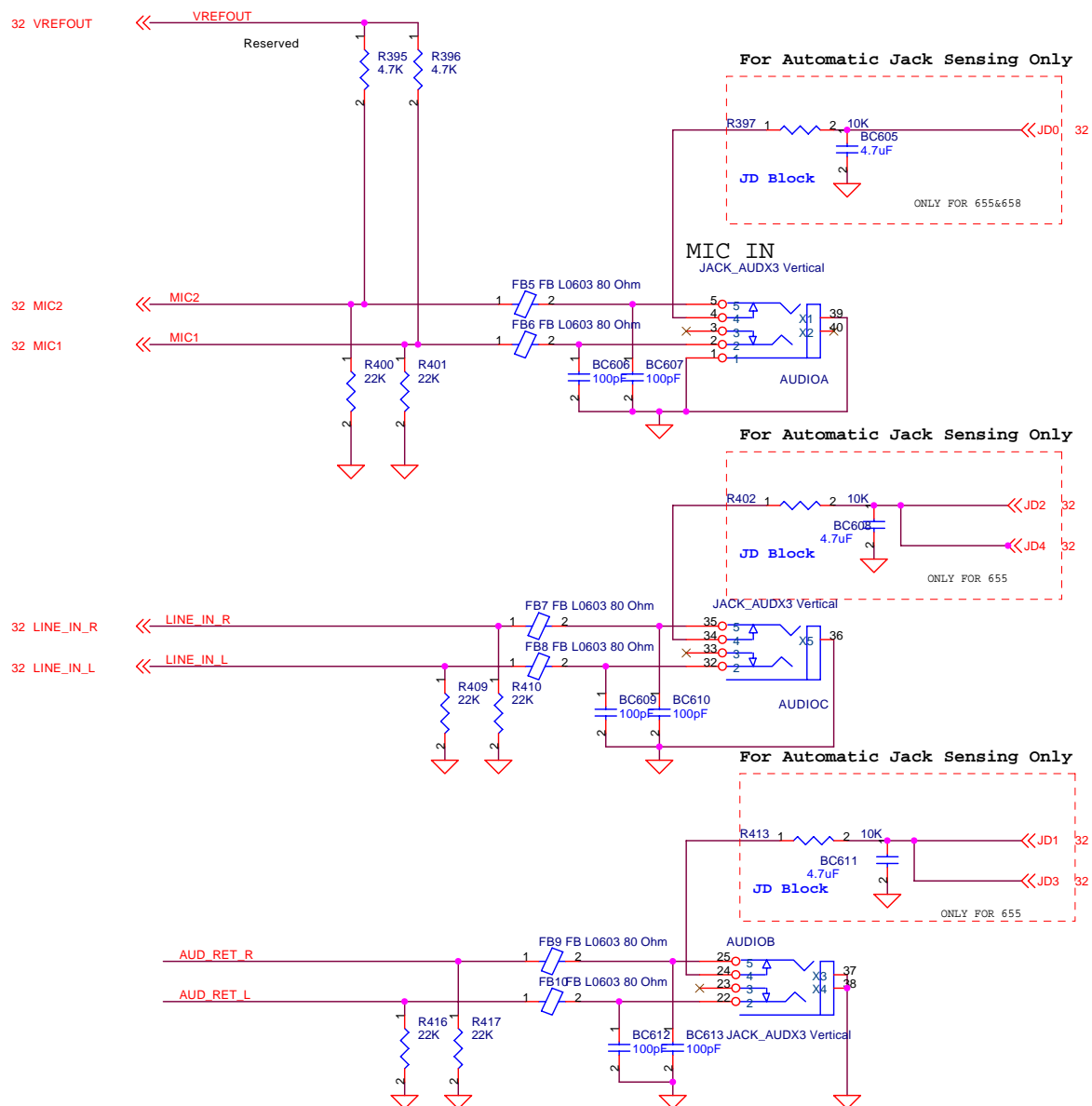
Rev
A

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ALC658 USE REALTEK FRONT PANEL



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FOXCONN PCEG

Title AC97 I/O

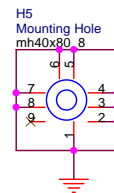
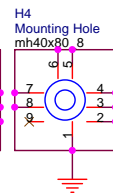
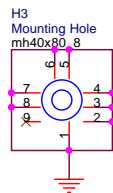
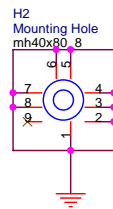
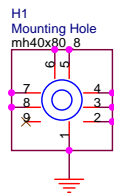
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Rev A

8 7 6 5 4 3 2 1

D D



C C



BULK POWER DECOUPLING

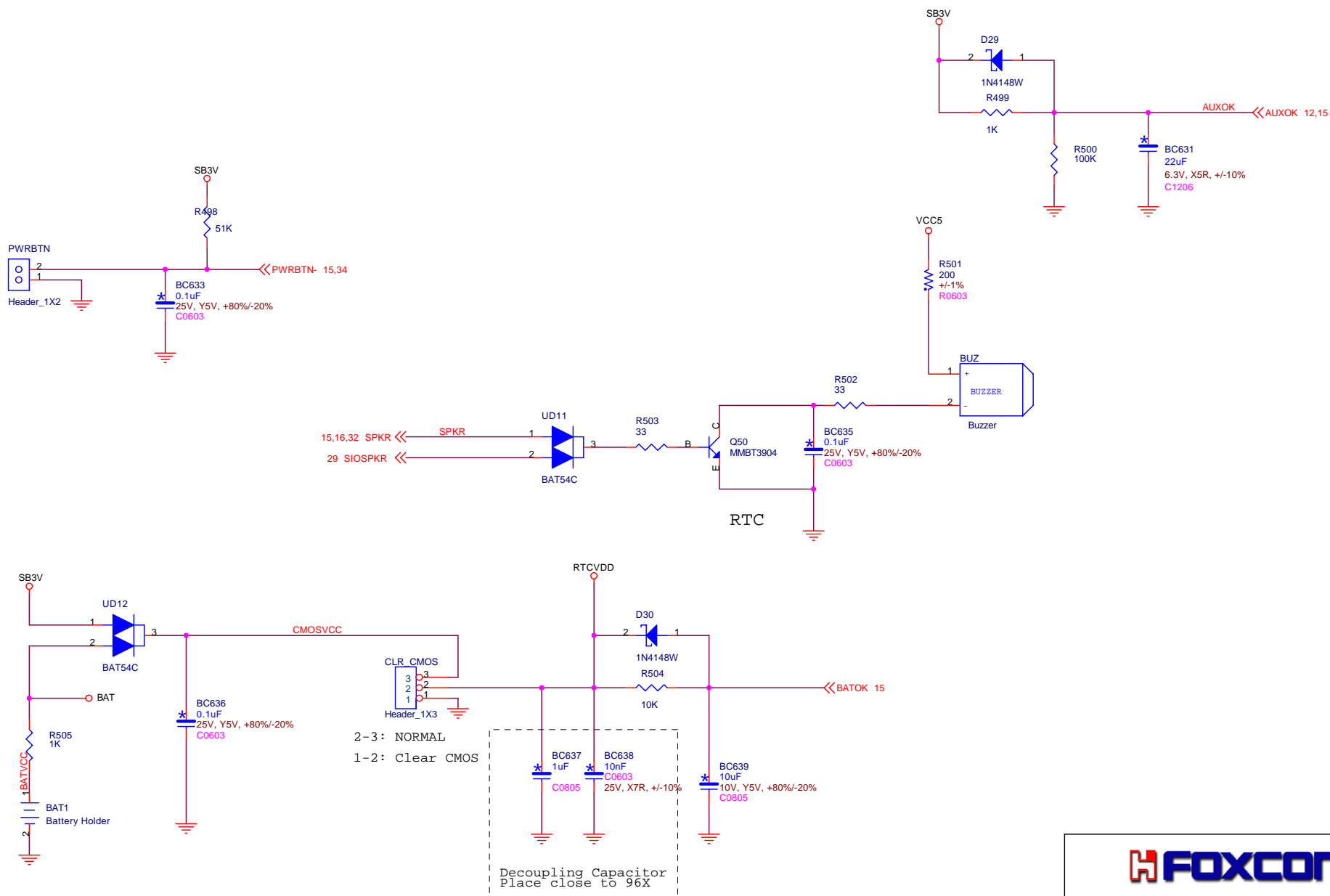
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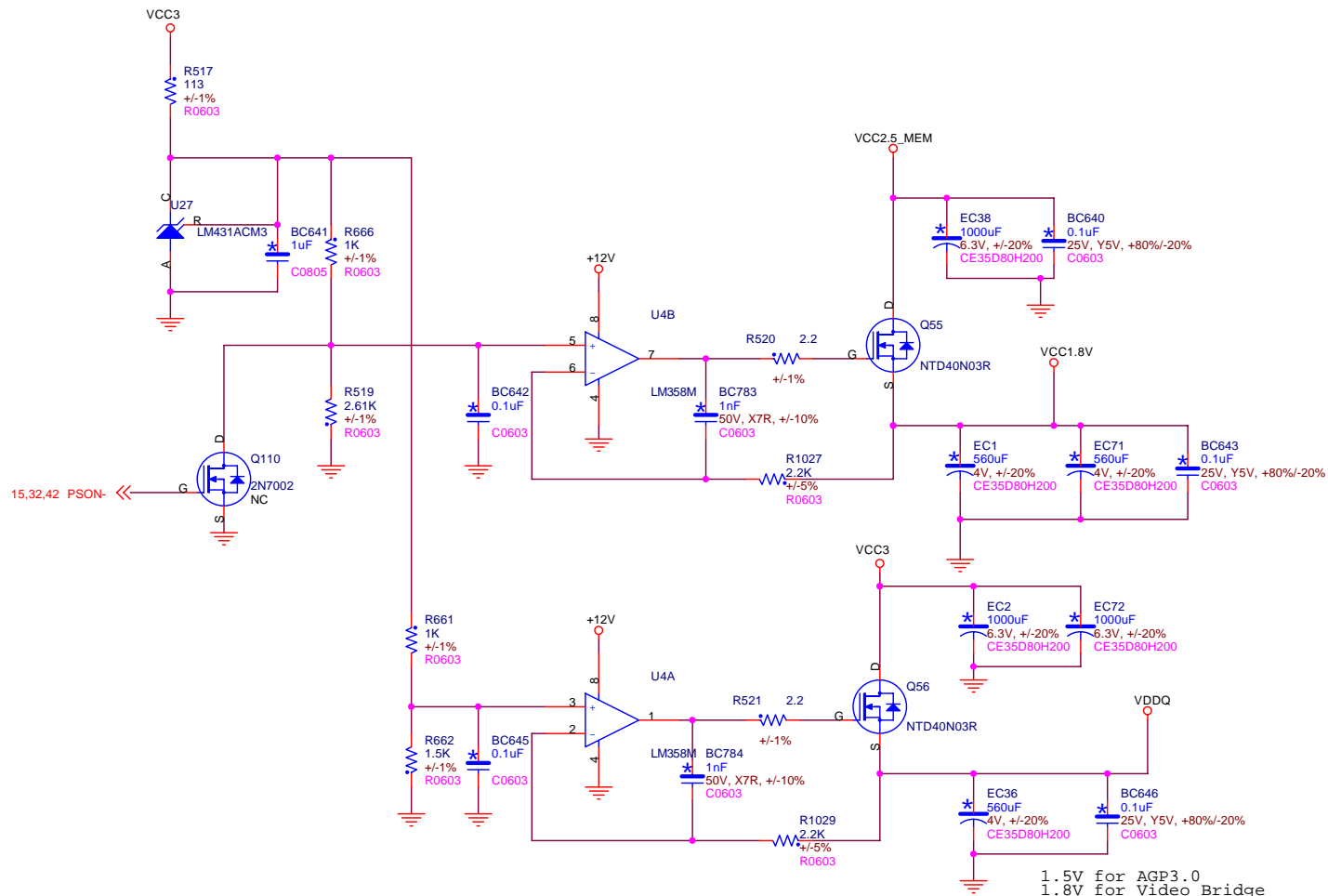


Title			POWER CONN	
Size	Document Number	661S01		Rev
Custom				A
Date:	Wednesday, September 22, 2004	Sheet	35	of 43



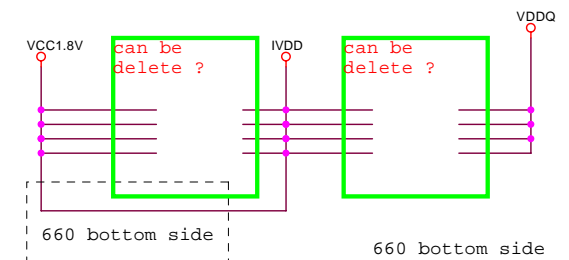


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1.5V for AGP3.0
1.8V for Video Bridge
VDDQ 1.8/1.5V

VBDT-	HI	LOW
VDDQ	1.5V	1.8V



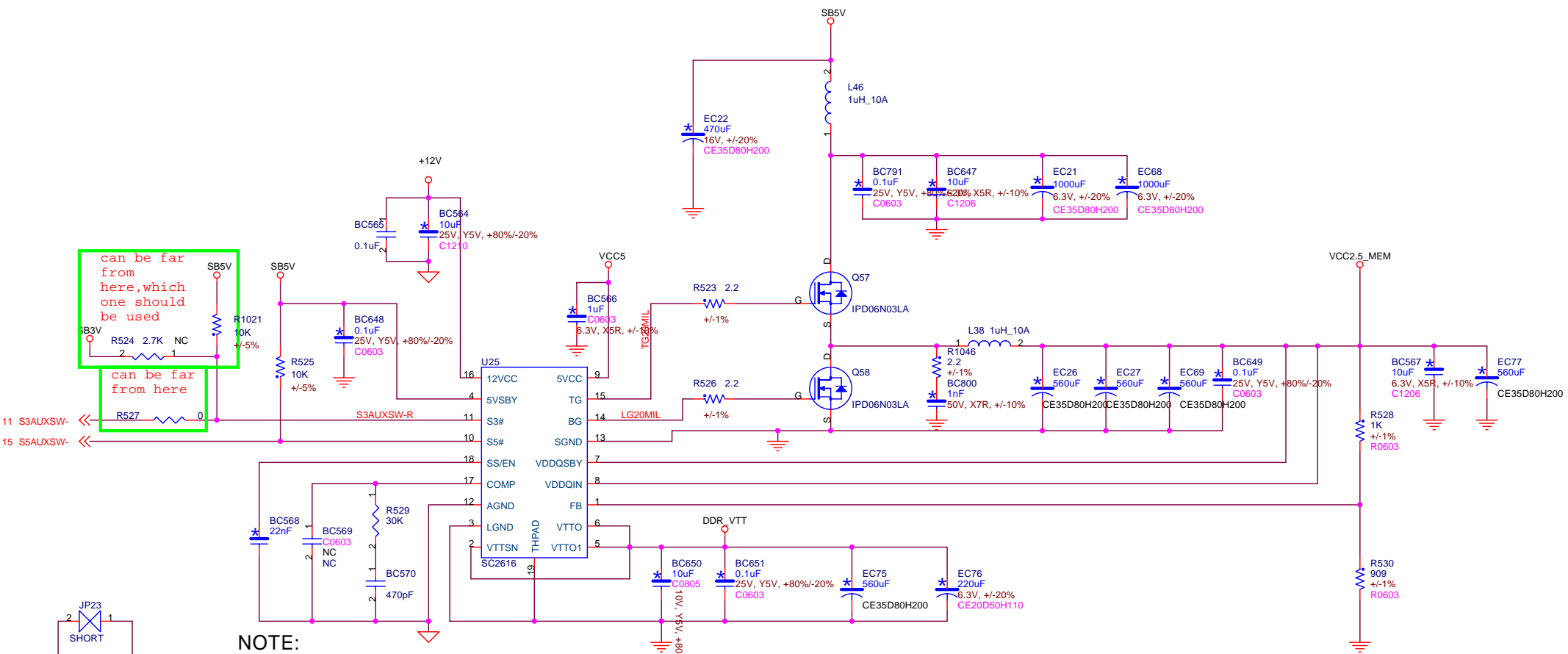
FOXCONN

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Title **POWER CONN**

Size Custom Document Number **661S01**

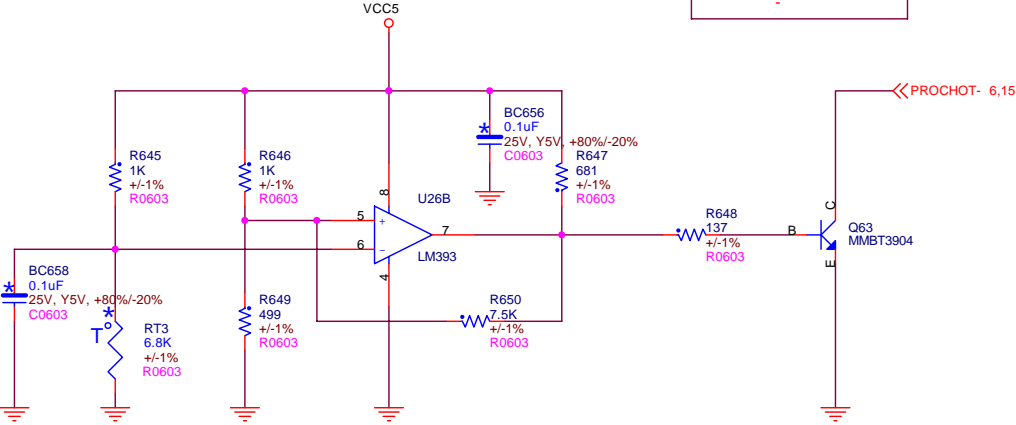
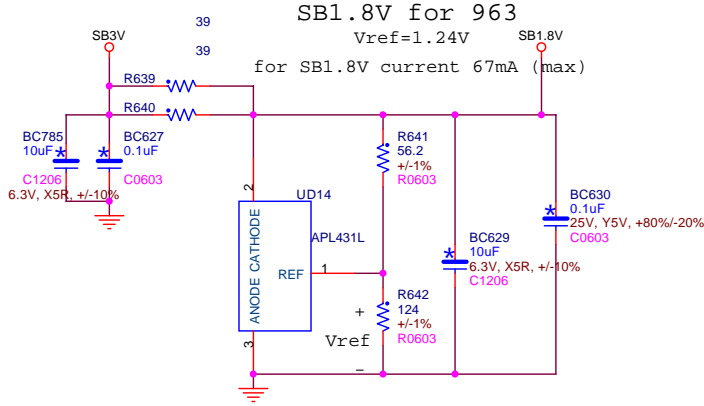
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NOTE:

1. Please be alerted for polarity of U2B. It's used for blocking reverse current from standby source to main source on mode S3.
2. R39 and R35 are necessary. S3# and S5# must be tied to 5Vstb to prevent them floating.

PROCHOTJ Signal



Reserve AUX_IVDD 1.5V for 660
Vref=1.24V
for SB1.5V current 48mA (max)

